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Analysis of Array Multiplier and Vedic Multiplier using Xilinx

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ABSTRACT
Many important signal processing systems are designed on VLSI platform as the integration growing rapidly. The signal processing systems and applications requires large computation capacity and hence takes considerable amount of energy. In the VLSI system design performance and area are the two very important parameters. Generally performance of any system is determined by the performance of the element that is multiplier. Multiplier is the slow element in the system. The two terms the area and speed are the main hurdles before the researcher because to improve the speed results in large area. As a result, while designing of multiplier with optimised speed and area is the major challenge. Therefore design of low-power multiplier has been an important area in VLSI system design research. Many researchers have been worked at circuit and logic, technology, physical level on designing low power, low area multipliers. The present paper deals with design and implementation of efficient high speed 16x16 multiplier using various algorithms like array & booth, and using Vedic operators. Multipliers are compared on the basis of optimized area, speed and memory required.

General Terms
Array multiplier Algorithm, Urudhva Tirayghybham Algorithm

Keywords
Multiplier, Area, booth, array multiplier, Vedic Multipliers

1. INTRODUCTION
In many arithmetic operation multiplication is the most important and basic operation. It is a fundamental block of multiplication based operations like ALU's, FFT's and Convolution and it also becoming an important part of digital filters. Many of the digital processing algorithms require high speed multipliers because execution time is very important parameter. Technology is developing towards the design of newer and high speed multipliers [4]. Speed, area and even combination of them are the key issues and challenge for the researchers in designing multipliers. For complex applications need of faster multiplier chip is high. It is also need of today to design and develop smart and effective multiplier algorithms that can easily implemented on chip. Some of the algorithms used in digital hardware are booth multiplication algorithm and array multiplication algorithm. These algorithms are associated with high propagation time. The fast multiplication Process is defined by Vedic Mathematics. The Veda means store of knowledge. The Vedic mathematics means storage of knowledge of mathematics related to the high speed operations. These Vedic mathematics provides the knowledge of varies area of mathematics like arithmetic, algebra, geometry using 16 important sutras. The method given in the Vedic maths is very simple. The Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884-1960) has combine all concepts together and given its explanation [1,6,8]. Out of 16 sutras the Urdhva-Tiryagbhyam Vedic Sutra, and Nikhilam Sutra are very much useful multiplication operation [2-5]. Present work is an effort to design and implement the multiplier using Urdhva-Tiryagbhyam Vedic Sutra [9], and Nikhilam Sutras and compare their performance with multipliers developed with booth algorithm and Array algorithm specifically in terms of area and speed. Many of the researchers have performed this operation in different ways. Harprit et.al has discussed a possible application of Vedic mathematics to digital signal processing in the light of application of Vedic multiplication algorithm to digital multipliers. A simple architecture based on the Urdhva Tiryakbhyam was used [9]. Purushottam D et.al. Highlighted the multiplication process and is implemented on 8085 and 8086 microprocessors, result shown big savings in processing time. It clearly indicates the computational effectiveness offered by Vedic operators [10]. Madhura Tilak et.al. Presented linear convolution there implementation improved the efficiency of the model design in terms of area and speed requirements. The system design is coded using VHDL language and synthesized for FPGA products with XILLINX 13.1 software [11]. Moses et.al.have examined how the Vedic algorithm of Urdhva Tiryakbhyam speeds up the computation of his algorithm when compared with conventional algorithms in existence [12].Khanhe and his team have developed and implemented floating point multiplier based on Vedic Multiplication Technique [13]. In this paper efforts have been made to design and implement multiplier using both the algorithms array and Urdhva-Tiryakbhyam Vedic Sutra. The comparative results are depicted in the paper.

2. EXPERIMENTATION

2.1 Design of Multiplier using Array Method
An Array multiplier has very common regular structure. An n bit Array multiplier has n x n array of AND gates to generate partial products, n x (n-2) full adders and n half adders. Each partial product bit is fed into a full adder which sums the partial product bit with the sum from the previous adder and a carry from the less significant previous adder. The number of rows in array multiplier denotes length of the multiplier and width of each row denotes width of multiplicand. `Design of Multiplier steps: The 16 * 16 bit array multiplier is simulated using Xilinx 8.1 tool. The design steps are as follows: Multiplier circuit is based on add and shift algorithm. Each partial product is generated by the multiplication of the multiplicand with one multiplier bit. The partial product are shifted according to their bit orders and then added. The addition can be performed with normal carry propagate adder. N-1 adders are required where N is the multiplier length.

				A3	A2	A1	A0	Inputs
			x	B3	B2	B1	B0	
			C	B0 x A3	B0 x A2	B0 x A1	B0 x A0	Internal Signals
		+	B1 x A3	B1 x A2	B1 x A1	B1 x A0		
		C	SUM	SUM	SUM	SUM		
	+	B2 x A3	B2 x A2	B2 x A1	B2 x A0			
	C	SUM	SUM	SUM	SUM			
+	B3 x A3	B3 x A2	B3 x A1	B3 x A0				
C	SUM	SUM	SUM	SUM				
Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Outputs

Figure1: Logic of Array Multiplier [18]

Algorithm:

1. Define variables for multiplier and multiplicand.
2. Use the shift and add method.
3. Cascade 4 blocks of 4x4 bit blocks together to form 16x16 bit multiplier.
4. The result of 16 x 16 multiplier will be 32 bits.

2.2 Design of Multiplier using Urdhva-Tiryakbhyam Vedic Sutra

The Urdhva Tiryakbhyam sutra is based on vertical and crosswise multiplication algorithm. Case Study II describes the use of this sutra to implement multiplier. This sutra enables the parallel generation of intermediate products and eliminates unwanted multiplication steps. This type of multiplier takes a form of one of the low power and high speed Multiplier. Design of Multiplier steps: The 16 × 16 bit Vedic Multiplier is simulated using Xilinx 8.1. The block diagram is as given below: The first step in the design of 16×16 block will be grouping the 8 bit (byte) of each 16 bit input. These lower and upper bytes pairs of two inputs will form vertical and crosswise product terms. Each input byte is handled by a separate 8×8 Vedic multiplier to produce sixteen partial product rows. These partial products rows are added in a 16-bit carry look ahead adder optimally to generate final product bits. The schematic of a 16×16 block designed using 8×8 blocks. The partial products represent the Urdhva vertical and cross product then using OR and half adder assembly to find the final product.

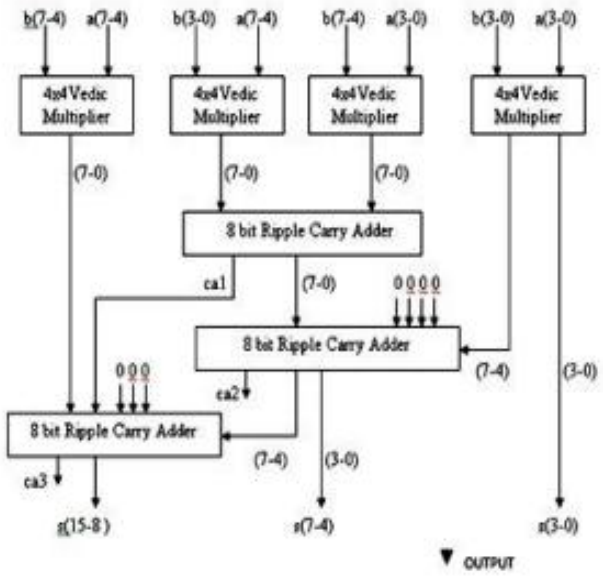

Figure2: Block diagram of Vedic multiplier [17]

3. SIMULATION RESULTS

Figure 1 shows the basic logic of Array multiplier. When the 16x16 bit data is multiplied using Xilinx 8.1 project navigator the details of the utilization of the design multiplier is shown below

Array Multiplier Device utilization summary:

Selected Device: 3s100evq100-5

Number of Slices: 290 out of 960, utilization is 30%

Number of 4 input LUTs: 505 out of 1920, utilization is 26%

Number of bonded IOBs: 64 out of 66, utilization is 96%

Maximum combinational path delay: 50.800ns

Total memory usage is 169844 kilobytes.

Figure 2 shows the basic logic of Vedic Multiplier. When the 16x16 bit data is multiplied using Xilinx 8.1 project navigator the details of the utilization of the designed Vedic multiplier is shown below

Vedic Multiplier Device utilization summary:

Selected Device: 3s100evq100-5

Number of Slices: 14 out of 960 1%

Number of 4 input LUTs: 25 out of 1920 1% Number of bonded IOBs: 16 out of 66 24% Maximum combinational path delay: 11.847ns Total memory usage is 150260 kilobytes

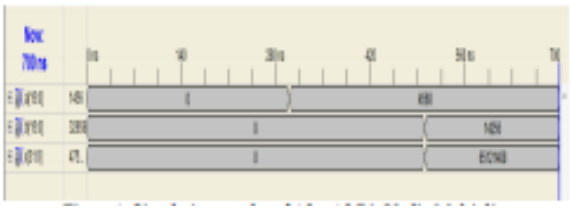

Figure3: Simulation results of 16 × 16 Bit Array Multiplier

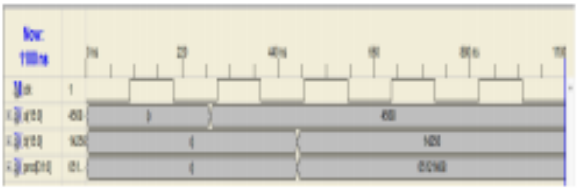

Figure4: Simulation results of 16 × 16 Bit Vedic Multiplier

4. COMPARISON OF MULTIPLIER FOR 16-BIT MULTIPLICATION

Table 1. Shows the comparison of the array and Vedic multiplier using various parameters like number of slices, number of 4 input LUT's Delay in ns and total memory usages

Parameters	Array multiplier	Vedic multiplier
Number of Slices	290 out of 960	20 out of 960
Number of 4 input LUTs	505 out of 1920	39 out of 1920
Delay in ns	50.800	9.710
Total memory usage in kb	184536	164120

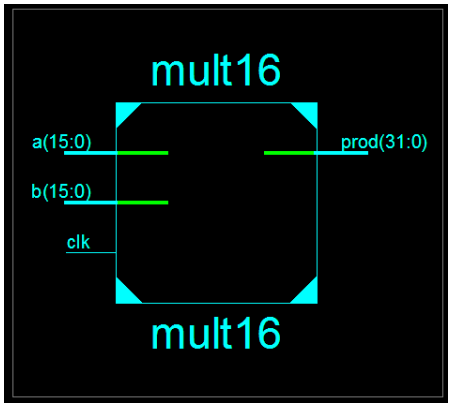

Figure: RTL Schematic of Array Multiplier

5. CONCLUSION

From the results it can be concluded that Urdhva-Tiryakbhyam Multiplier is giving good performance with respect to speed, delay, area, complexity and power consumption. The use of Vedic multiplier can be explored to design and implement efficient high performance multipliers. This type of multiplier if used in realization of digital IIR and FIR filter in VLSI then the performance of filters may improve.

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