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Low Power High Speed Multiplier Design based on MTCMOS Technique

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ABSTRACT
The need for devices that consume minimum amount of power was a major driving force behind the development of CMOS technologies. Reduction of power consumption makes a device more reliable. As a result, CMOS devices are best known for low power consumption. Most research on the power consumption of circuits has been focused on the switching power and the power dissipated by the leakage current has been comparatively minor area. Today, every designer either analog circuit or a digital circuit designer is concerned about the amount of power consumption in the circuit at the end. Multi-threshold CMOS is becoming a trendy circuit design technique for low power, high performance application. The paper briefs the implementation of a novel CMOS 8 bit Vedic Multiplier using MTCMOS.

General Terms
PTL (pass transistor logic), Low power, Multiplier.

Keywords
MTCMOS (Multi threshold CMOS), Sub-threshold leakage current, Vedic Mathematics, Urdhva Tiryagbhyam Sutra.

1. INTRODUCTION
In recent years, there has been fast growth in battery-operated portable applications such as notebook and laptop computers, personal digital assistants, cellular phones, and other portable communication devices. These devices which remain in the standby state for a significant time interval demand for reducing the standby sub-threshold leakage power tremendously [1]. Also, scaling of technology and supply voltage, leakage power has become significant in power dissipation of Nano-scale CMOS circuits. Hence computation of leakage power is critical in designing of low power circuits to enhance performance [2]. To minimize leakage power dissipation in sleep mode, a significant circuit technique is proposed such as Multi-threshold voltage CMOS (MTCMOS). The demand for multipliers is continuously increasing in the fields like Signal Processing and fields involving high speed processors. Multipliers are implied in Digital Signal Processing and Image Processing. They are widely used in the hardware implementation of Discrete Fourier Transform, Discrete Cosine Transform, and Discrete Sine Transform and telecommunication and broadband communication industries. Multiplication is the process of adding a number of partial products. Multiplication algorithms differ in terms of partial product generation and partial product addition to produce the final result [3]. Multiplication requires carry propagation from the least significant bit (LSB) to the most significant bit (MSB) during the addition of binary partial products thus the latency incurred is during the addition and subtraction of the binary products formed after multiplication [4].Vedic mathematics is the ancient methodology of Indian mathematics which has a unique technique of calculations based on 16 sutras (Formulas). A high speed multiplier design using Vedic Mathematics principals is presented in this paper. Also, the add/subtract units are adopted from "Vedas". On basis of those formulas, the partial products and sums are generated in one step which reduces the carry propagation from LSB to MSB. The implementation of Vedic multiplier and their application to the complex multiplier ensure substantial reduction of propagation delay in comparison with conventional array architecture and parallel adder based implementation.

2. SUB THRESHOLD CURRENT DISSIPATION
Sub-threshold leakage current flows in MOS transistors when the gate voltage V_{GS} is below the threshold voltage of the MOS transistor. When V_{GS} is larger than V_{TH}, majority carriers are repelled from the gate area of the transistor and a minority carrier channel is created. This is known as *strong-inversion*, as more minority carriers are present in the channel than majority carriers. When V_{GS} is lower than V_{TH}, there are less minority carriers in the channel, but their presence comprises a current and the state is known as *weak-inversion*. At $V_{GS}<V_{TH}$, an N-channel MOSFET is in the off-state. However, an undesirable leakage current can flow between the drain and the source. The MOSFET current observed at $V_{GS}<V_{TH}$ is called the **sub-threshold leakage current**. This is the main contributor to the MOSFET OFF-state current, I_{OFF}. This is the drain current Id measured at $V_{GS}=0$ and $V_{DS}=V_{DD}$. It is important to keep I_{OFF} very small so as to minimize the static power that a circuit consumes even when it is in the standby mode. Sub- threshold leakage can be expressed as below:

$$I_{SUB} = W/L\ \mu V_{TH0}{}^2 C_{sth} \exp\left(\frac{V_{GS}-V_T+\eta V_{DS}}{nV_T}\right)(1-e^{-VDS/V_T})$$

Where W and L denote the transistor width and length, μ denotes the carrier mobility, V_T =KT/q where K Boltzmann constant and the thermal voltage T, $C_{sth} = C_{dep}+C_{it}$ denotes sum of depletion region capacitance and interface trap capacitance η is DIBL coefficient and n is slope shape factor as n= C_{sth} /C_{ox} [5]. C_{ox} is the gate input capacitance per unit area of the MOS gate. Putting it together the leakage current of an OFF transistor is given by following equation.

$$I_{OFF} = I_{REV} + I_{GIDL} + I_{SUB}$$

Where I_{SUB} is the dominant component because I_{REV} and I_{GIDL} are maximum when $V_{DB} = V_{DD}$.

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For short channel devices, I_{SUB} increases with V_{DB} due to DIBL (drain induced barrier lowering) effect.

3. POWER DISSIPATION REDUCTION

3.1 Standby Leakage Reduction

Battery powered devices remains idle for most of the time except when in use. However, since the phone remains on, it drains power from the battery which reduces battery life. In such a situation, battery power can be saved by shutting down the power supply to the circuit when not in operation. Techniques falling into this category cut-off the circuit from the supply rails when the circuit is in idle state [6].

3.2 Multi-threshold CMOS

Multi-threshold CMOS is an increasingly popular circuit approach that enables high performance and low power operation [7]. Multi-threshold CMOS technique reduces leakage current during idle modes by providing a high threshold "gating" transistor in series with the low V_{TH}, circuit transistors, creating the virtual path between the supply and the ground. In active mode, the high V_{TH}, transistor is turned ON whereas in sleep mode it is turned OFF, providing a small sub-threshold leakage current. For an entirely combinational circuit, where state need not be preserved, only one type of high V_{TH}, device is actually required. The NMOS is preferable because it has a lower ON resistance and can be sized smaller than a corresponding PMOS sleep transistor [8]. Such a structure using NMOS transistor is applied in proposed multiplier design shown in Figure1: MTCMOS Structure.

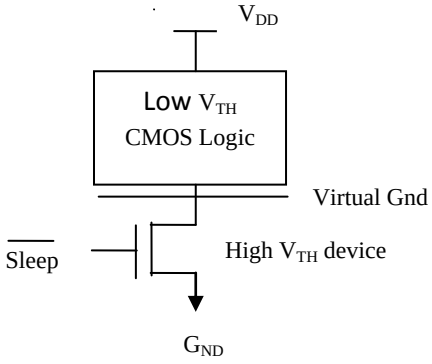

Figure 1: MTCMOS structure

4. VEDIC MATHEMATICS

4.1 Vedic Sutra (Rules)

Vedic mathematics minimizes typical calculations in conventional mathematics to very simple one. Since, Vedic formulae are said to base on the natural principles on which the human mind functions. Arithmetic rules of Vedic Mathematics allow more efficient speed implementation in field of computing. One such useful rule called is: **Urdhva Tiryagbhyam Sutra.** It is a general multiplication formula applicable to all cases of multiplication. It literally means "*Vertically and Crosswise*". The algebraic principle of this rule is based on multiplication of polynomials. Here, both Partial product generation and addition is performed concurrently. Hence, it is adaptive to parallel processing [4].

4.2 Multiplication by using Urdhva Tiryagbhyam Sutra

The example shows how multiplication is done using this rule.To find the product of two digit numbers 14×12 steps are as follows:

i) The right hand most digit of the multiplicand, the first number (14) i.e., 4 is multiplied by the right hand most digit of the multiplier, the second number (12) i.e., 2. The product 4×2 = 8 forms the right hand most part of the answer.

ii) Now, diagonally multiply the first digit of the multiplicand (14) i.e., 4 and second digit of the multiplier (12) i.e., 1 (answer 4 × 1=4); then multiply the second digit of the multiplicand i.e., 1 and first digit of the multiplier i.e., 2 (answer 1×2 = 2); add these two i.e., 4 + 2 = 6. It gives the next, i.e., second digit of the answer. Hence second digit of the answer is 6.

iii) Now, multiply the second digit of the multiplicand i.e., 1 and second digit of the multiplier i.e., 1 vertically, i.e., 1 so 1×1 = 1. It gives the left hand most part of the answer. Thus the answer is 168. The process is explained symbolically as seen in Figure 2: Multiplication (14×12) by Urdhva Tiryagbhyam Sutra. The symbols are operated from right to left.

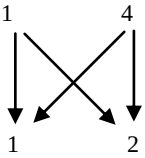

Figure 2: Multiplication (14×12) by Urdhva Tiryagbhyam.

4.3 MTCMOS Vedic Multiplier

The 2×2-bit Vedic multiplier is structured by using four AND gates and two Half Adders as shown in Figure: 3 2×2 MTCMOS Vedic Multiplier. The 1st Half Adder is used to add outputs of AND gates having input A1B0 & A0B1 and 2nd Half Adder are used to add carry generated from 1st Half Adder and output of AND gate having input A1B1. The implementation of multiplier design is performed using 90nm CMOS technology in Tanner EDA 13.0v tool.

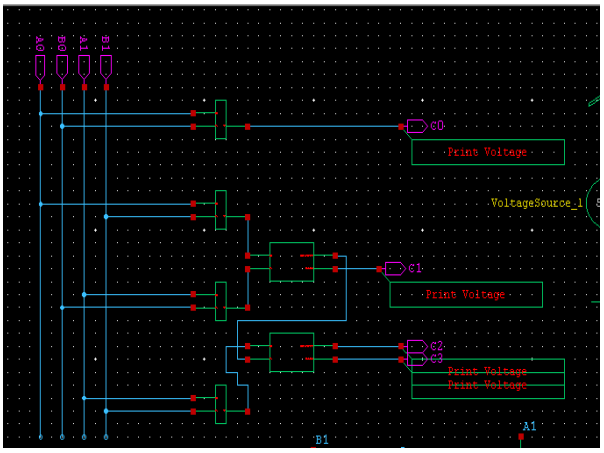

Figure 3: 2×2 Vedic Multiplier Block Schematic

In similar manner 4×4 Vedic multiplication, which multiplies two 4-bit numbers (A and B), where each number can be

expressed as (A0–A3, B0– B3); A3 and B3 being the most significant inputs by using the 2×2 multiplier block [4].

The block diagram in Figure 4: 4×4 Vedic multiplication blocks below shows product of 4 bit numbers. Each square block in the diagram represents a 2×2 bit Vedic multiplier unit. First 2×2 bit Vedic multiplier has inputs as A1A0 and B1B0. The last block is also 2×2 bit Vedic multiplier with inputs A3 A2 and B3 B2. The blocks in the middle are 2×2 bit multipliers with inputs A3 A2 & B1B0 and A1A0 & B3 B2. So to obtain final product (s7 s6 s5 s4 s3 s2 s1 s0), four 2×2 bit Vedic multipliers and three 4-bit Carry Look Ahead (CLA) Adders are required.

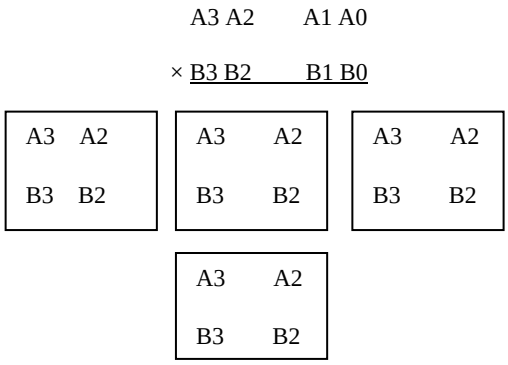

Figure 4: 4x 4 Vedic multiplication blocks

4.3.1 Carry Look Ahead adder

A carry look-ahead adder improves speed by reducing the amount of time required to resolve carry bits [9]. The carry look-ahead logic uses the concepts of generating and propagating the carry bit. The sum (S_i) is implemented in three stages to avoid delay mismatching with the carry generation [10]. Figure 5: 4 bit CLA adder shown below is used in designing the multiplier. The expression of the i^{th} sum and the $(i + 1)^{th}$ carry output can be given as below:

$$S_i = A_i \oplus B_i \oplus C_i$$

$$C_{i+1} = A_i B_i + (A_i \oplus B_i) C_i$$

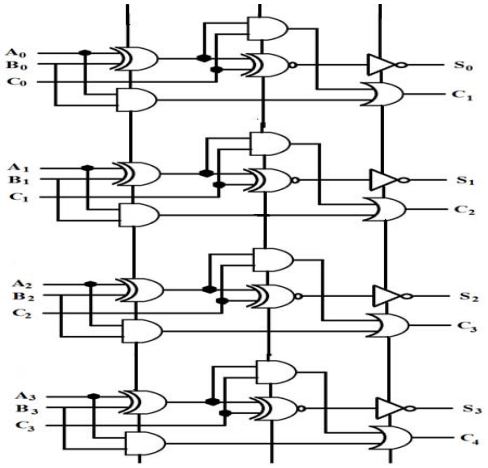

Figure 5: 4 bit CLA adder

Similar style is used to construct 8 bit CLA. The proposed carry look ahead Adder is designed using CMOS technique and it performed with less propagation delay as compared to ripple carry adder [11]. Comparison of delay and average power of CLA and RCA adders is shown in Table 1.

Table 1. Comparison between delay and average power of CLA and RCA adder [11]

Adder Design	Average Power (watt)	Delay (sec)
Carry Look ahead	1.369×10^{-3}	3.187×10^{-8}
Ripple carry Adder	4.871×10^{-4}	4.857×10^{-8}

4.3.2 8×8 Vedic Multiplier (MTCMOS)

The 8x8 bit Vedic multiplier can be implemented by using four 4×4 bit Vedic multiplier modules [4]. The input bits are (a7- a0) and (b7-b0) the resulting multiplication's 16 bits output will be bits (s15-s0). This structure uses four 4×4 bit Vedic multipliers and three 8 bit CLA adders (having 2 inputs of 8 bits) as per the design requirement. Inputs are applied to the 4×4 bit Vedic multipliers and the output of multiplier is of 8 bits. Now, the input of the first CLA adder is the output of the 2nd and 3rd 4×4 bit multipliers which gives output of 8 bits (7-0) plus one carry. The second CLA adder adds the output of first CLA adder (7-0) with the 4 bits (7-4) that is the output of 1st 4×4 Vedic multiplier and remaining 4 bits of the adder are considered as 0 (dummy variable) because of reduced results. So output is of 8-bits (7-0) and one carry (carry is discarded). The 3rd CLA adder adds the output of 4th 4×4 bit multiplier (7-0) and 4 bits of output of 2nd CLA adder (7-4); other 4 bits are carry bits of 1st CLA adder and 0. Hence, the output of 8×8 multiplier is s(3-0) output of first 4×4 bit multiplier(3- 0), s(7-4) is output of 2nd CLA adder (3-0) and s(15-8) is output of 3rd CLA adder (7-0). The block structure of implemented multiplier is shown in Figure 6: 8×8 Vedic Multiplier Block Schematic.

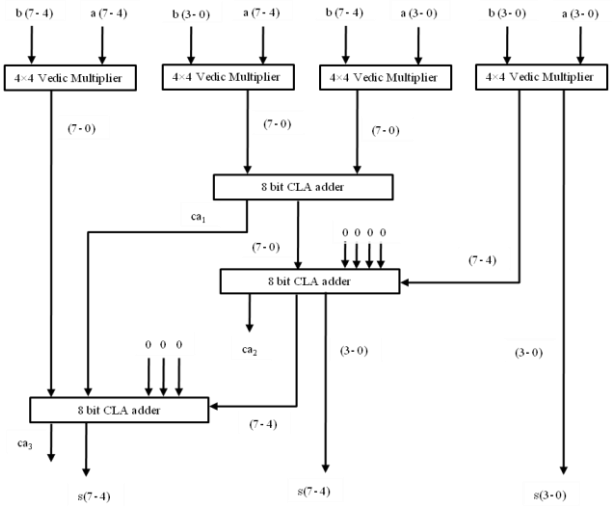

Figure 6: 8×8 Vedic Multiplier Block Schematic

The Implementation schematic of 8×8 vedic multiplier using MTCMOS technique is shown in the Figure 7: 8x8 MTCMOS vedic multiplier.

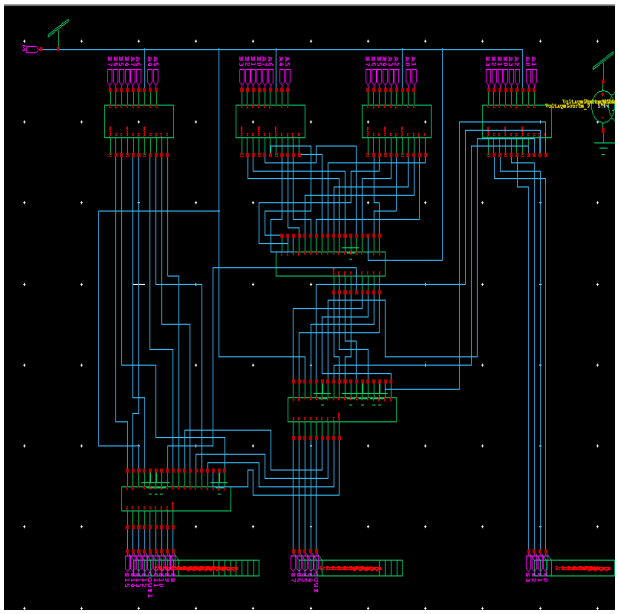

Figure 7: 8×8 MTCMOS vedic multiplier.

The transistor level implantation of Vedic multiplier is carried out by first implementing the transistor level schematic for half adder and then using this half adder implementation to create full adder, implementing 2×2 vedic multiplier, 4x4 multiplier and then integrating them to form 8 bit vedic multiplier. To implement this 8×8 vedic multiplier using MTCMOS technique 32 half adders, three 4 bit CLA adders and three 8 bit CLA adders were required. When compared with conventional static CMOS vedic multiplier implementing RCA adder the proposed design showed 24.92% reduction in area (number of transistors). Also, the PTL implementation of vedic multiplier showed less average power consumption and 31.26% reduction in area as compared with conventional static CMOS vedic multiplier.

5. CONCLUSION

Power consumption, delay, speed, chip area are some of the key concerns in the VLSI industry today. Reduction in the power consumption and delay of a multiplier circuitry is expected to cause a revolution in the field of electronics and communication as these circuits are widely used in every digital and analog system including computers, calculators and other electronics commodities. Furthermore, the design can be improved by using combination of two logic styles static CMOS and PTL (Pass Transistor Logic) called as Hybrid PTL/CMOS logic. Also, theVedic multiplier and CLA adder used for addition can be modified with adiabatic logic and can be useful in more power saving.

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