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Implementation of FPGA based D.C motor Speed Controller using PWM Technique

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ABSTRACT
The speed controlling of a DC motor drive using field programmable gate array (FPGA) as a digital controller, which provides an operational control using PWM technique. Mostly switching power converters are employed to deliver the energy to the motor. Pulse width modulation is one of the good ways of control that delivered energy through power Mosfet. The P.W.M signal is given from the F.P.G.A board through the Mosfet driver circuit. The presented work is programmed on FPGA board Altera D.E 2.0.FPGAs flexible architecture reduces the processing speed, accuracy, robustness and hence increases the overall systems efficiency. The integration of all these above mentioned resources led to successful implementation of D.C motor P.W.M speed controller using FPGA and furthers more since dynamo has been coupled with motor to behave as load resulted in achieving the open loop control system for a generator of 206watts.

General Terms
Pulse Width Modulation, Control System, FPGA, Verilog HDL.

Keywords
PWM, FPGA, D.C motor speed control, Dynamo.

1. INTRODUCTION
One of the ways of designing a digital speed control system for D.C motor is based on software. In order to run that software microprocessor, PLC, DSP can be used. These all above mentioned software based techniques employees' memory processor interaction. The memory holds the application program while the processor fetches decodes and executes the program instructions. The implementation of speed controlling using microprocessor and DSPs is old and well known [1], [2].When the system size and complexity increases; Application Specific Integrated Circuits are utilized. The ASIC must be fabricated on a manufacturing line

, a process that takes several months ,before it can be used or even tested[3].With the passage of time digital controllers are taking new shapes and in this connection another development in this regard was of FPGA.FPGAs are configurable ICs and used to implement logic functions.

Early generation of FPGAs were most often used as glue logic which is the logic needed to connect the major components of a system. They were often used in prototypes because they could be programmed and inserted into board in few minutes. Today high end FPGAs can hold several millions gates and have some significant advantages over ASICs. They ensure ease of design, lower development costs, more product revenue and the opportunity to speed products to market. At the same time they are superior to software based controllers As they are more compact, power efficient, while adding high speed capabilities [4].

Moreover, FPGAs flexible architecture allows the implementation of many complex systems that requires parallel execution. These systems may range from pattern recognition to security algorithms as they have complex architecture [5], [6], [7], [8].

Before implementing the P.W.M speeds controlling method for motor. A test bench was achieved by controlling the speed of the motor using PIC microcontroller. Apart from the thorough literature review is done of the control system, digital control system, P.W.M, encoder and FPGA cyclone II board. The mentioned literature topics are studied from book and as well as resources from internet.

P.W.M speed controlling method is programmed on the FPGA. The P.W.M signal of 100Hz is transmitted from GPIO_0 (0) to the D.C gear motor via motor driving circuit. The energy that switching power converter a DC motor is controlled by Pulse Width Modulation signal applied to the gate of a power mosfet.The motor is coupled with the dynamo and a load back comprises of resistive bulbs are connected in series, to obtain sharp observance of the changes due to variation in speed of the motor. Since as the speed of the dynamo coupled motor increases the intensity of the bulb increases and viceversa.An encoder is coupled on the shaft of the motor for giving feedback pulses of the speed of the motor to the FPGA board on pin GPIO_0 (1) .The encoder has measured the feedback pulses for the duration of 1Hz.Keys on the FPGA board are used to vary the duty cycle of the input P.W.M signal and it's also displayed on seven segment of the board. In addition to this the seven segments are also displaying the speed of the motor which is coming from the feedback path by encoder. Apart from that graphs between speed of the motor and the duty cycle of the PWM signal at a constant voltage of 7V have been drawn and shown here. This was done to proceed further with the project to make it a close loop system with 7V as a set point.

2. CONTROL SYSTEM
Control system is defined as an interconnection of components to provide a desired system response [9]. Classical and modern controlling methods were created in 19the century, a revolution came when control system is transformed and used into latest technologies such as motor control applications. Unlike close loop control system, open loop control systems do possess accuracy, robustness, good performance and stability. Furthermore it's cost effective and the design is less complex as compared to close loop control system.

2.1 Digital Control System

It is a type of control system that employees computer as a digital controller. As per the need of the application the digital controller can take the shape of microcontroller, microprocessor, dip's and FPGA etc. Since digital control system is discrete in nature this field of technology in mid

1960s and mid-1970s, had replaced mainframe computers which were previously controlling numerous control applications such as (motor speed control).

Admiring this fact, a similar effort is done in such a way that the FPGA; a product from the evolution of embedded system has been chosen as digital controller for the purpose speed control, as showing the figure1 below.

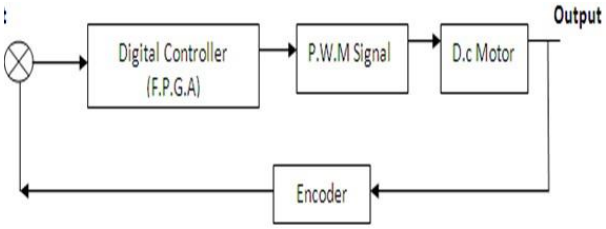


Figure1.control system block diagram for speed control of motor using FPGA

2.2 Pulse Width Modulation

These days' industries are increasingly demanding process automation in all sectors. Automation marks into better quality, increased production and minimized cost. The variable speed drives, which can control the speed of A.C/D.C motors, they are essential controlling elements in automation systems. According to the need of the applications, several of them are fixed speed and rests are of variable speed drives. The concept of pulse width modulation is the varying of the amplitude of the pulse width by varying the duty cycle of signal or pulse [10].

Since the energy is provided inform of pulses for short duration of time. It is their fore In comparison to other methods of speed controlling the P.W.M is found to be generating less amount of heat, the motor consumes less energy and as well as offered finer control over motor.

3. HARDWAREDESIGN

Foremost step that was taken in the hardware was a selection of a D.C gear motor. D.C gear motor has gear attached to its shaft. It helps in determining the speed and torque of the motor with load and no load [11]. The motor is operating at 36V.See table1 for the technical specifications of the dc motor, taken from its datasheet. [12].

Table1. D C motor specification

Model	dc/V	I/A	Speed/rpm	I/A	Speed/rpm
Da061ga304	0-100	0.56 No load	560 No load	3.58 Max efficiency	560 Max efficiency

A permanent magnet Dynamo has been chosen as a load, for the D.C motor. Dynamo has been extracted out from the generator found in cars. The dynamo is couple with D.C gear motor by the lathe machine operator. The coupling is done in such a way that the radius of the pulley of the motor (4.5inches) is three times greater than the pulley of the dynamo(1.5inches).Both of the pulleys are connected with the pulley belt of size A-36 inches. The difference in sizes of the pulley has been done to increase the speed of the motor and as expected it did increase the speed of the motor, causing

The dynamo to generate more A.C voltages. This is followed by the designing of motor driving circuit.

The purpose of the circuit was to drive the motor when the P.W.M signal generated form FPGA. It has three major components named as anon-inverting amplifier LM741 [13], Mosfet IRF 3205[14] and TP4N35 [15] Opto-coupler along with passive components and a schotkey diode [16] in parallel with the motor for protection. See the table2 below for the components functions.

Table2. Components function

Component	Function
Lm741	To amplify The PWM signal from 2V To 8V.
TP4N35	To provide electrical isolation between Mosfet and motor for feed forward signal and to work as signal conversion between encoder and FPGA for feedback signal.
IRF 3205	To drive the motor when receive signal from FPGA, has VDC=55V& Idss=110A
610MIC	A safety diode for protection of the motor, low leakage current (100micro amp) and low Vfd=0.9V.

Positive edge of PWM signal is amplified by the non-inverting amplifier. Than it passes through the Opto coupler; the collector current of the Opto- coupler shorts the gate of the Mosfet which drives the motor on the desired speed depending on the width of the PWM signal. Using multiuse software the circuit was tested before implementation. The schematic of the motor driving circuit is given below in f ig3.

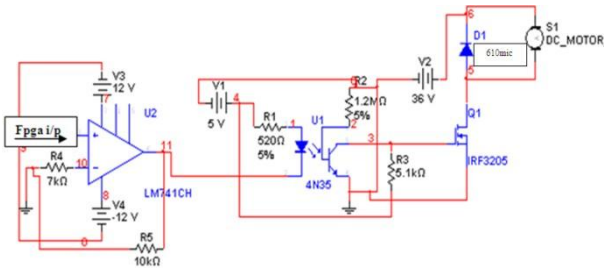


Figure2. Motor driving circuit

A resistive load bank consisting of 28 bulbs has been designed and is in series connection with the dynamo. Out of these 28 bulbs, 18 bulbs are of rating (10W/12V) while 10 bulbs are of rating (5W/12V).Toggle switches are being used to turn the bulbs of the load bank ON & OFF.A cooling fan for ventilationpurposesisusedwhichisoperatingat12V.Two D.C

power supplies are used, named as primary and secondary power supplies. Primary power supply of 36V designated to motor whereas a secondary power supply (which is giving

5V, 12V,-12V, 5V) is used to provide 12V to encoder of the motor and to the cooling fan, 12V and -12V for the non-inverting amplifier in the motor driving circuit. After completing these all segments of hardware implementation, a portable wooden box has been made to contain all the hardware involved in the box.

Dynamo coupled motor has been placed inside and fixed permanently; the load bank came on the top along with the Toggles switches and panel meters (digital A.C ammeter and voltmeter to display current and voltages of the load respectively at the load on corresponding speed of the motor.)Seefig3below

Figure3.Portablewooden box

3.1 Encoder Interface

A digital optical encoder is a gadget that converts motion into a sequence of digital pulses [17].By counting as in glebitor by decoding a set of bits. These pulses can be transformed to obtain relative or absolute position measurements. Linear and rotary configurations are found in encoders, but the most general type is rotary. Rotary encoders are made in two basic forms: the absolute encoder where an exclusive digital word corresponds to each rotational position of the shaft. The incremental encoder produces digital pulses when shaft rotates. It allows the measurement of relative position of shaft. Optical encoder major advantage is that it offers high resolution.

In the presented work the incremental encoder is coupled directly to the motor's shaft, instead of mounting it and it saved space too. Initially encoder wire is connected to shaft of motor, but air gap was created. A Crim shell connector has been used to avoid any problem of air gap in future. On full scale RPM the encoder was giving (3.2 KHz) so it was scale down to (100 Hz) for making processing easy. However the Encoder output than was of (7V) and frequency (3.69

KHz).This was a bit problem because the used FPGA board was operating at 3.4V.It is their fore an opt coupler was used as a signal conversion ,it brought down the output of encoder form 7V to 4.6V.Furthermore a voltage divider circuit is designed The purpose was to bring down the output voltages of encoder form 4.6V to 3.46V.Because the FPGA board is operating at 3.46V(See fig4).The FPGA programming is performed under the encoder module (see flow chart below) which count pulses of the feedback signal from the encoder of the motor for the duration of 1Hz.

As the positive edged pulses from the encoder will be feedback to the GPIO_0 (1) pin of the FPGA board the frequency will undergone an increment of 10 on every count (this increment was done for making frequency readable).If the duration reached to 1Hz (see fig5.1) the counted pulses saved in variable frequency will be assigned to a new variable named as width and will be displayed on the seven segment display as the speed of the motor. Resulting in successful measuring of the speed of the motor from the encoder (see fig 5.2).

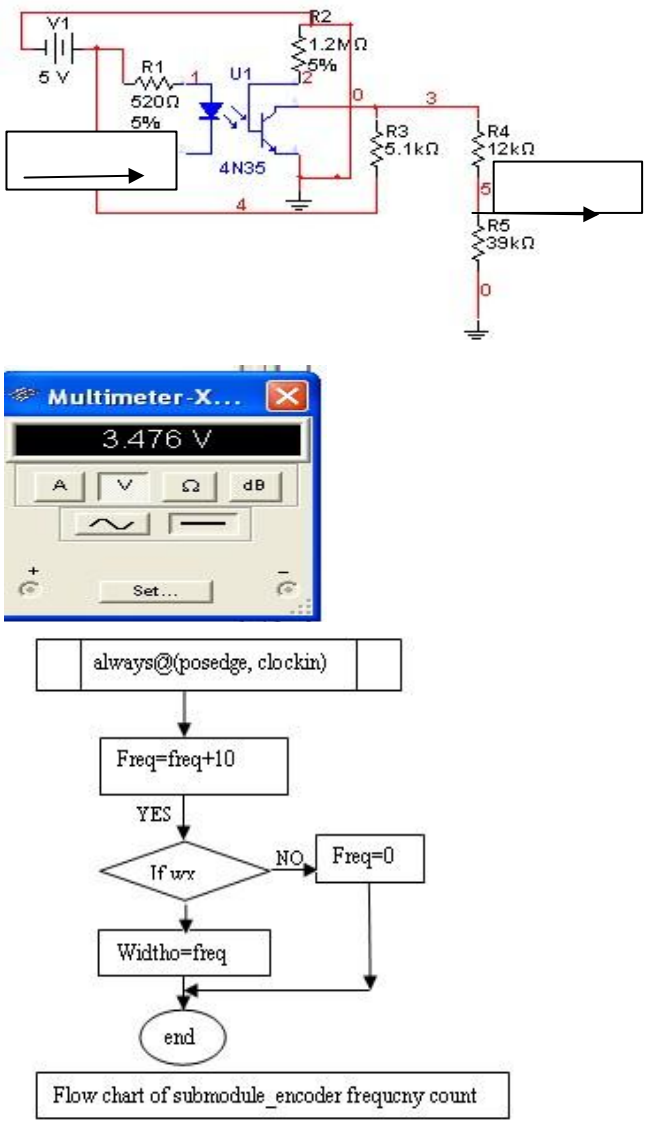


Figure5. 1 Flow chart of encoder module

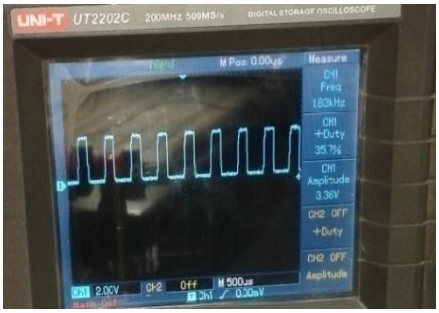


Figure5.2.Square wave pulses from the encoder.

4. FPGA ALTERA CYCLONE

Cyclone [18], FPGAs are based on stratix architecture, but are intended for low cost applications. There are three generations of these devices, called cyclone II and Cyclone III.A cyclone chip has the same basic structure as of (stratix LAB,Dsp and memory blocks courtesy of Altera).Inaddition,ithasa4- Input LUT logic element that has dedicated erythematic circuitry and a programmable flip flop. The types of memory blocks provided in these devices are M4K in cyclone. Cyclone II devices also includes DSP blocks and range in size from

2910 to 119,088 logic elements and 4Mbits of memory.

4.1 Application

Modern FPGAs and their distinguishable capabilities have been advertised extensively by FPGA vendors .Moreover, few referred articles addressed and advantages of utilizing these powerful chips[19][20].In the past two years FPGA families have been successfully utilized in a variety of applications which include inverters[21][22],communications[23],embedded processors[24] and image processing[25].

4.2 Quartus II VerilogHDL

A useful source of information for writing Verilog HDL is Quartus software [26].The help feature of Quartus includes the description of Verilog features and contains tutorials with a text editor tool [27].It's a very convenient guide to Verilog syntax.

4.1 FPGA IMPLEMENTATION

The Fpga implementation contains Verilog HDL programming for generating PWM signal. The main module of the program consists of different blocks of coding and different sub modules for (seven segment display, clock divisions). The whole programming in the main module program and is execution parallel processing.

4.2.1 Creation of a G.U.I

A G.U.I has been created for the interaction between the user and the FPGA board. It contains the declaration inputs and outputs (such as keys, switches, clock 27MHz) and initialization of used variables etc. See fig below.

```
input [17:0] SW;                                  reg [39:0] GPIO_0,GPIO_1;
input [3:0] KEY;                                  reg [17:0] LEDR;
input CLOCK_27;
inout [39:0] GPIO_0,GPIO_1;                       integer count=0;
output [17:0] LEDR;                               integer freq=0;
output [3:0]LEDG;                                 integer a=0;
output [7:0]                                      integer b=0;
HEX0,HEX1,HEX2,HEX3,HEX4,HEX5,HEX                 integer loop=0;
6,HEX7; integer tenth, unit,fp1,fp2;              integer width=0;
Integer tentho,unito,fp1o,fp2o;                   integer widtho=0;
wire w1,w2 ,w3 , wx  ;
```

Figure6.Coding of G.U.I

4.2.3 Seven Segment Display sub module

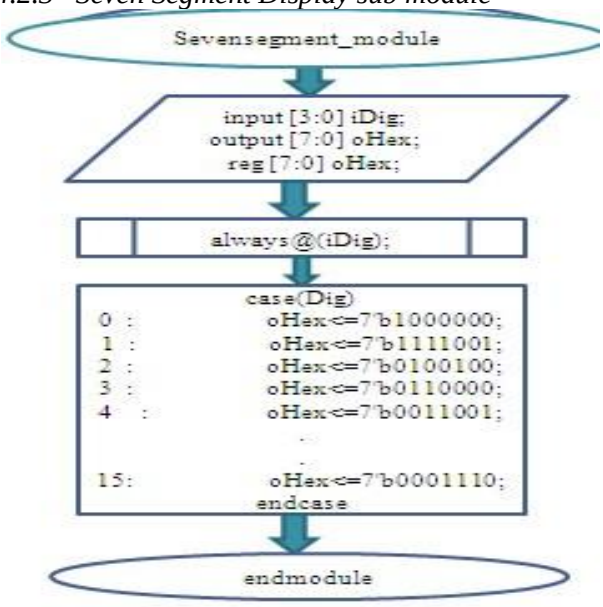


Figure7.Flowchartofseven segment display

4.2.2 Clock Division Sub Module

The FPGA board has a built in clock of 27 MHz .It has been brought down to1MHz to generate the required PWM signal of 100Hz.Seeflow chart in fig6.

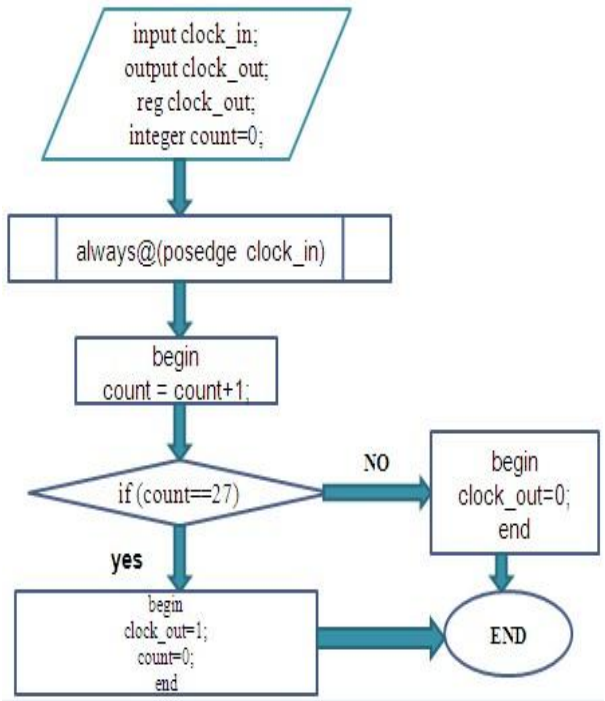


Figure8.Clock division to obtain 1 MHz

Figure 9 shows a flow chart displaying the creation of 100Hz PWM signal using at GPIO_0 [0] of FPGA board. Figure 8 shows the digital oscilloscope showing the PWM wave of 100Hz.

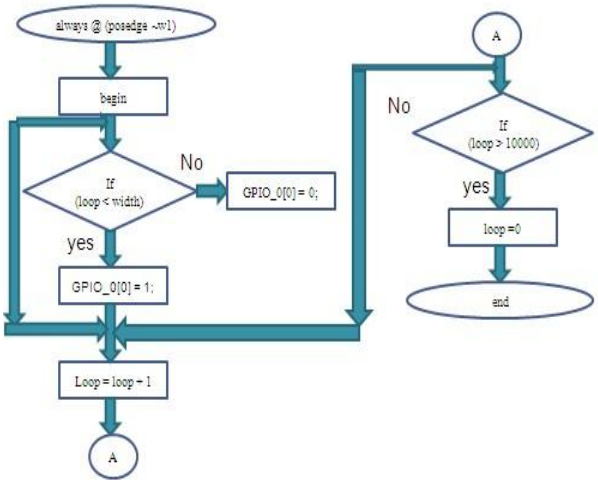


Figure9. 1MHz PWM signal

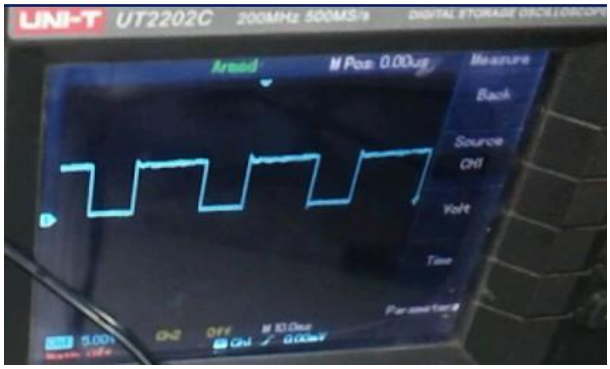


Figure10.PWMwaveof 100Hz on the digital oscilloscope.

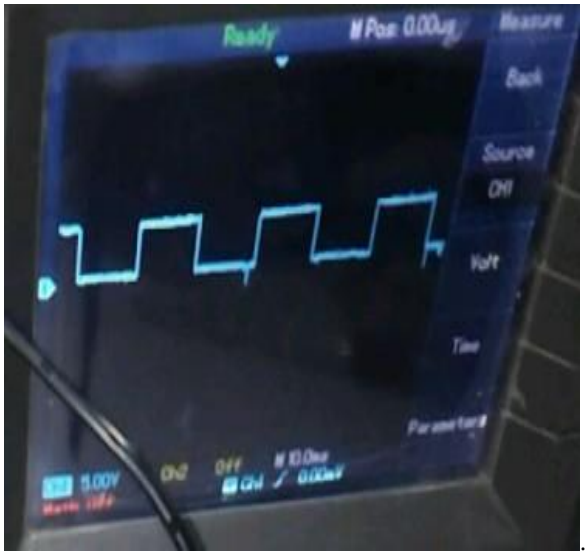


Figure11.PWM signal on the O/P of Mosfet.

4.2.3 Coding for measuring the duty cycle.

```
//Duty cycle of the input signal
SEVEN_SEG seg0(HEX0,fp2);
SEVEN_SEG seg1(HEX1,fp1);
SEVEN_SEG seg2(HEX2,unit);
SEVEN_SEG seg3(HEX3,tenth);

// Encoder freq
SEVEN_SEG seg4(HEX4,fp2o);
SEVEN_SEG seg5(HEX5,fp1o);
SEVEN_SEG seg6(HEX6,unito);
SEVEN_SEG seg7(HEX7,tentho);
```

```
always
begin
Tenth = (width-width%1000)/1000;
Unit  = (width-width%100-tenth*1000)/100;
fp1   = (width- width%10 - 1000*tenth-100*unit)/10;
fp2   = (width-1000*tenth - 100*unit - 10*fp1);
End
always
begin
Tentho = (widtho-widtho%1000)/1000;
Unito  = (widtho-widtho%100-tentho*1000)/100;
fp1o   = (widtho- widtho%10 - 1000*tentho-100*unito)/10;
fp2o   = (widtho-1000*tentho - 100*unito - 10*fp1o);
End
```

4.2.4 Key interface

The Fpga board has four keys. Four of them are being used in this presented work for the purpose of varying the width of the PWM signal as per desire of the user. This module handles the bounce effect of the pushed key and adjusts the cycle of the pushed key till the period of time it is being pressed. See the flow chart on figure10.

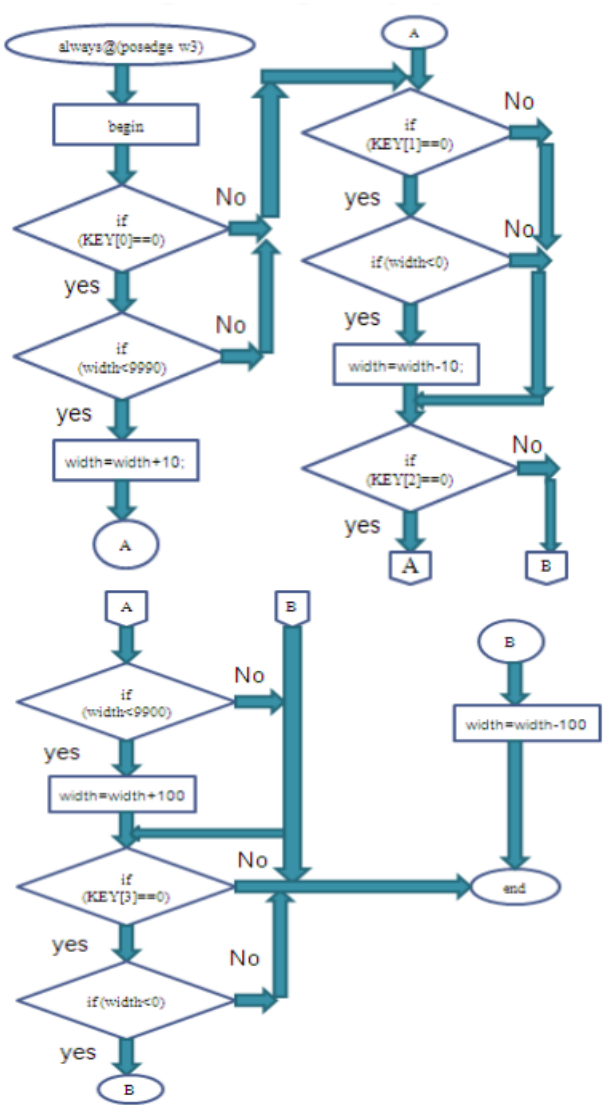
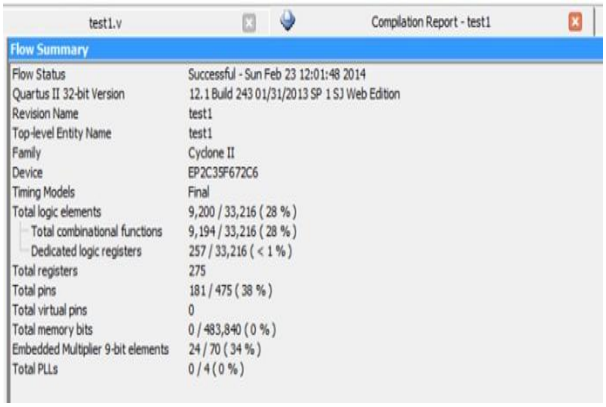


Figure12.keysinterfaceprogram for varying the PWM Signal from Fpga board

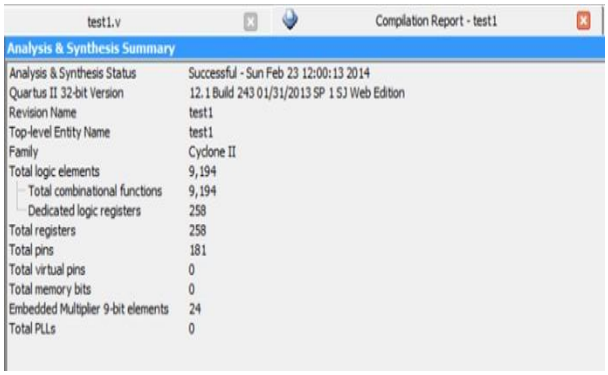


test1.v — Compilation Report - test1

Flow Summary

Flow Status	Successful - Sun Feb 23 12:01:48 2014
Quartus II 32-bit Version	12.1 Build 243 01/31/2013 SP 1 SJ Web Edition
Revision Name	test1
Top-level Entity Name	test1
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Total logic elements	9,200 / 33,216 (28 %)
Total combinational functions	9,194 / 33,216 (28 %)
Dedicated logic registers	257 / 33,216 (< 1 %)
Total registers	275
Total pins	181 / 475 (38 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	24 / 70 (34 %)
Total PLLs	0 / 4 (0 %)

Figure13.Flow summary of program



test1.v — Compilation Report - test1

Analysis & Synthesis Summary

Analysis & Synthesis Status	Successful - Sun Feb 23 12:00:13 2014
Quartus II 32-bit Version	12.1 Build 243 01/31/2013 SP 1 SJ Web Edition
Revision Name	test1
Top-level Entity Name	test1
Family	Cyclone II
Total logic elements	9,194
Total combinational functions	9,194
Dedicated logic registers	258
Total registers	258
Total pins	181
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	24
Total PLLs	0

Figure14.Anaylsis & synthesis summary of program

5. RESULTS

The result section features the operation of the system as a whole. The operation initiates with the power supply connections to the hardware. The designed program of controlling the D.C motor is burned via usb blaster cable on to the FPGA board Altera D.E 2.0.The seven segments on the FPGA board are initialize to zero. Since the power supplies have been turned ON the digital ammeter and digital a.c voltmeter also initialized to zero. Using the keys on FPGA board the duty cycle of the PWM signal is made to increase which causes the dynamo coupled motor to run.

5.1 PWM Speed Control Dynamo Coupled Motor with no Load Bank

Using the keys of the Fpga board the duty cycle of the PWM

Signal is made to increase to its maximum value which is 99.9%.It was observed that while increasing the duty of the PWM signal the speed of the dynamo coupled motor increases.

Similarly again using the key on the Fpga board the width of the PWM signal was made narrow. This caused decrement in the speed of the dynamo coupled motor.

5.2 PWM Speed Control of Dynamo Coupled Motor with Load Bank

This test gives a more enhanced observance of the variation in the speed of the dynamo coupled motor as now the bulbs of the load bank will be drawing in the generated voltages from the dynamo to flow the current in them in order to achieve brighter state of intensity.

The duty cycle of PWM signal was increased, the speed of dynamo coupled motor increases and since the load bank was ON, the bulbs were glowing brighter and brighter and it is also evident from thefigure15a&bbelow.

Figure15a.Full brightness on increasing PWM signal

When the duty cycle of the PWM signal was decreased the speed of dynamo coupled motor decreases and since the load bank was ON, the bulbs were glowing less bright and it is also evident from the figure below.

Figure16a.Less brightness on increasing PWM signal

Figure16b.Low PWM signal

During the conduction of test with load bank, alarge number of readings were taken of load current, frequency of the motor at different load (usually the load was greater than the precedent load on every turn). While keeping the dynamo coupled motor's generated voltage at 7V.In doing so when the desired voltage drops from 7V, the duty cycle of the PWM signal was increased (which increases the width of the PWM signal).The increment in the duty cycle increases the speed of the motor, hence supplying enough energy to dynamo coupled motor for maintaining7Vonthe output irrespective of the amount of load. It is important to mention here that the full load was of 28 Bulbs.7V load voltage was successfully maintained on full load with the help of PWM speed controlling technique.

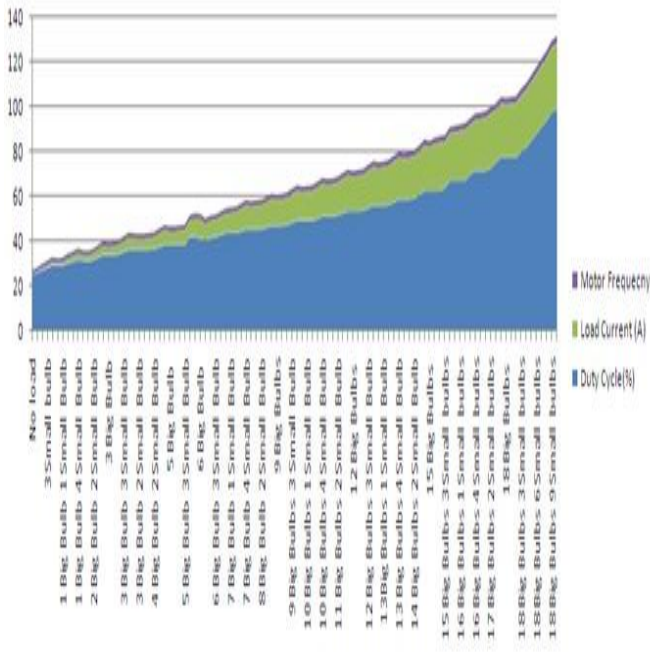


Figure17.A 2-Dchart

A huge number of readings have been plotted on graphs which shows t he relationship between speed of the motor andthe duty cycle of PWM signals (see fig18), load current and duty cycle of PWM signal (seefig19) and encoder frequency against duty cycle of the PWM signal(seefig20).As seen from the graphs the red line indicates that a linear relationship couldn't been achieved Their fore it was made Linear by doing the regression analysis of the data collected for plotting graphs. This led in achieving the open loop control system for a speed control of a D.C motor using PWM technique. The collected data has been saved on excel sheet and it can be easily viewed and downloaded from the web link www.tinyurl.com/ieeg-projects

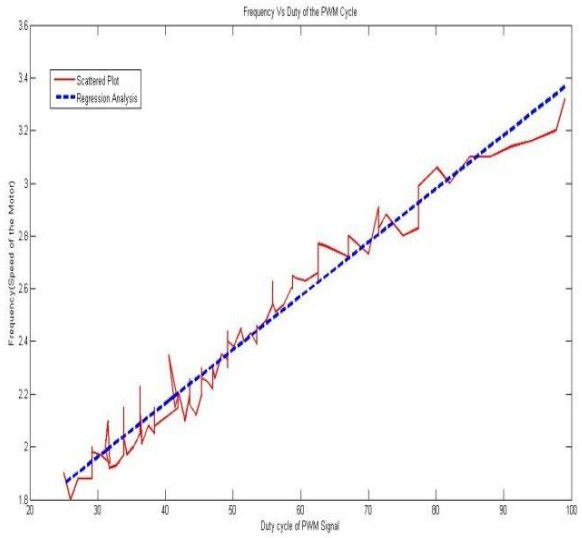


Figure18.Speedof motor VS duty cycle of PWM

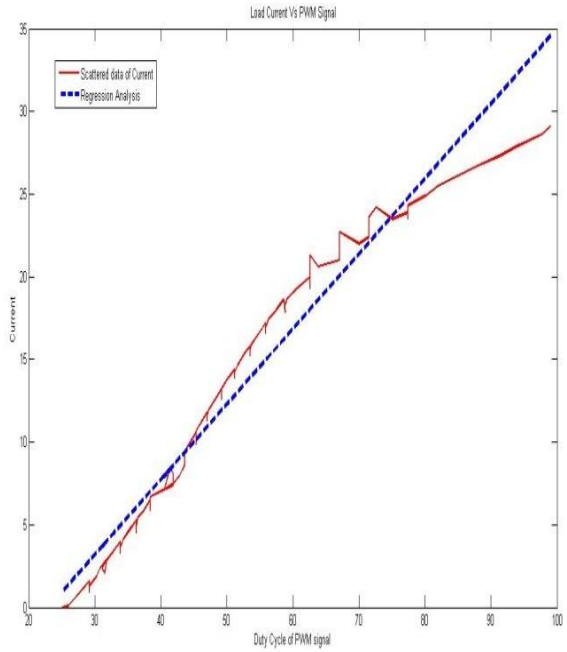


Figure19:Duty cycle of PWM vs. frequency of motor.

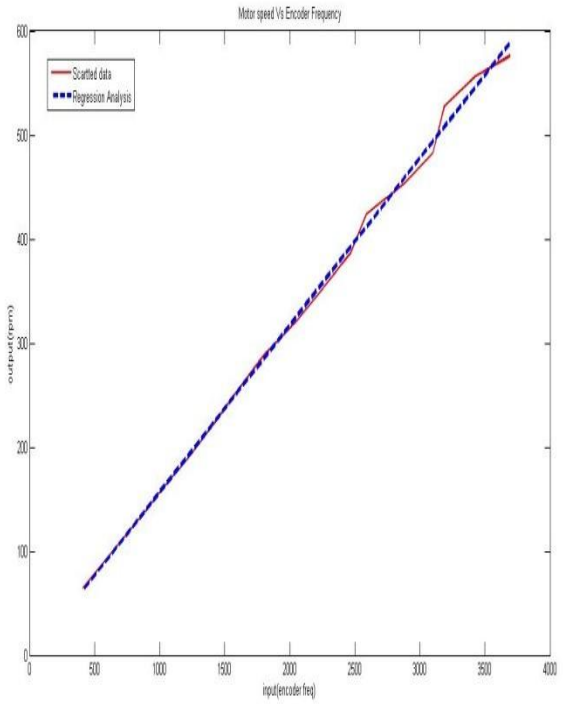


Figure20.Speed of the Motor VS Encoder Output

6. CONCLUSION

In the current era of high speed and high density, Fpga provide viable design alternatives to dsp, microprocessor and ASIC based applications. FPGA offer the most ideal approach of designing PWM technique for motor control applications. When design is implemented on FPGA they are designed in such a way that they can be easily tailored if any need arise in

future. Writing code on Verilog HDL is easy and simple, they can be well understand in short period of time .FPGA based PWM controller for speed control of DC motor is fast, accurate, and robust [28].The design is not complex as several external circuits like for keypad interface or seven segment display not needed to implement, they are already available on Fpga board. This whole system can be further studied and converted into a PID controller for DC motor.

7. ACKNOWLEDGMENTS

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