Reversible Logic Synthesis of Modulo Operation using an Optimized Parallel Binary Adder/Subtractor

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ABSTRACT
Reversible logic is gaining importance in recent years largely due to its property of low power consumption. It has a wide range of applications which include advance computing, low power CMOS, optical information processing, quantum computing, DNA cryptography and nanotechnology. Reversible gates are the building blocks of quantum computation. This paper presents an optimized parallel binary adder/subtractor using existing reversible gates which is further used to implement a novel circuit capable of performing modulo operation. All circuits have been modeled and verified using Verilog and Modelsim. An overall analysis of the modulo circuit and a comparative study of the proposed parallel adder/subtractor with respect to previous designs in terms of the number of gates, number of garbage outputs and quantum costs is presented.

General Terms
Reversible logic, Quantum Cost, Reversible Gates, Reversible Modulo Operation, Reversible Parallel Binary Adder/Subtractor.

Keywords
Reversible logic, Power consumption, CMOS, Nanotechnology, Reversible gates, Modulo operation, Parallel binary adder/subtractor, Garbage Output.

1. INTRODUCTION
As Moore's law continues to hold, miniaturization of integrated chips continues to take place. This leads to more power dissipation. Cumulative reduction of chip size will eventually lead to quantum dimensional components. Conventional logic circuits dissipate heat energy during their operations. These circuits perform irreversible computations which results in loss of information and it was shown by Landauer that this information loss dissipates kTln2 amount of heat. On further investigation Bennet[1] showed that information is lost when the input vector cannot be uniquely recovered from its output vectors and the energy dissipated is directly linked with the number of bits lost. Heat dissipation can be prevented if reversible circuits are used. Information loss can be prevented if the input bits can be completely recovered from the output. Hence the property of reversibility[1][2], will be an important aspect in future circuit design and it is important to realize technology that is capable of operating at such atomic levels while following the property of reversibility to ensure low power dissipation.

However, reversible logic[4][5][6][9][13] is suffering from two problems. Firstly, there is a shortage of technology with which reversible gates[12][13] can be built. Work is continuing in this field. Secondly, though a lot of research is being done on how to design combinational circuits using reversible logic, less work is being done in the area of sequential reversible logic implementations [3][13][14][15][16][17]. There is no limitation inherent to reversible logic, preventing the design of sequential circuits; in fact when Tommaso Toffoli first characterized reversible logic in his 1980 work 'Reversible Computing' he stated that "Using invertible logic gates, it is ideally possible to build a sequential computer with zero internal power dissipation".

1.1 Reversible Logic Synthesis
A reversible circuit[12][13] is a circuit in which the number of output vectors is equal to the number of input vectors and there is a one to one mapping between each input and output vector. For example let an input vector I_V and an output vector O_V be defined as follows:
$I_V = (I_1; I_2; I_3; I_i, :I_n)$
$O_V = (O_1;O_2;O_3; O_i;:O_n)$

Then $I_j \leftrightarrow O_j$, $\forall$j and j=1,2,3,i,..n

1.1.1 Cost Metrics
The cost metrics in logic circuits include the quantum cost, delay and the number of garbage outputs.

1.1.2 Quantum Cost
The quantum cost of circuit is defined in terms of the number of primitive gates used.

1.1.3 Garbage Output
The number of unused or unwanted outputs which are obtained to satisfy the condition of reversibility is called the garbage output.

2. BASIC QUANTUM GATES
2.1 Feynman Gate
Also known as the Controlled NOT Gate or CNOT Gate[12][13],this gate is a multi-qubit gate and also one of the most important quantum gates. Any quantum circuit can be implemented using only this gate and this gate is considered the universal gate for a quantum circuit. It consists of a control and target qubit. The value of the target is changed depending on the value of the control. The quantum cost of CNOT Gate is 1.Two input vectors A and B are mapped to the

corresponding output vectors P and Q. Here, the input A is the control which determines whether the target input B is to be complemented or not through the XOR operation.
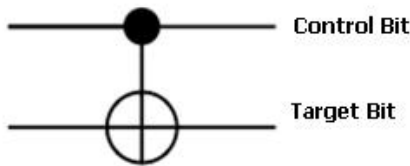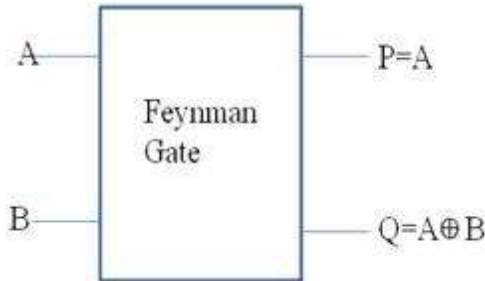

Fig 1: CNOT Circuit

Fig 2: CNOT: Block Diagram

The Double Feynman Gate is similar to the Feynman Gate in operation but has an extra input vector. Correspondingly the quantum cost is 2.The block diagram of Double Feynman gate is shown below.
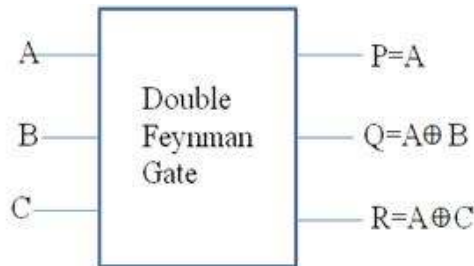

Fig 3: Double Feynman Gate

2.2 Toffoli Gate

The Toffoli Gate has a quantum cost of 5.The relation between the input vector I(A,B,C) and output vector O(P,Q,R) is shown in the figure below. The AND and NAND operations can be realized using this gate and hence any classical circuit can be implemented using this gate.
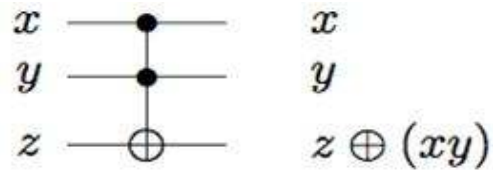

Fig 4: Toffoli Block Diagram

Fig 5: Toffoli Circuit Diagram

2.3 Fredkin Gate

Similar to the Toffoli gate, it has a quantum cost of 5 and the input and output vectors I(A, B, C) and O(P, Q, R) are related as shown in the figure below.

Fig 6: Fredkin Gate Block Diagram

The Fredkin gate[12] can be used to swap the inputs at the output or to perform the if-else condition. In the above figure, if the value of A=1, then Q=C and R=B. Hence the inputs get swapped at the output. There is also a 4-input Fredkin gate, whose block diagram is shown below. The quantum cost of the 4 input Fredkin Gate is 5.

Fig 7: Block Diagram of 4-Input Fredkin Gate

2.4 BJN Gate

The BJN Gate has a quantum cost of 5 and the relationship between the input vector I(A,B,C) and output vector O(P,Q,R) is shown in the figure below.
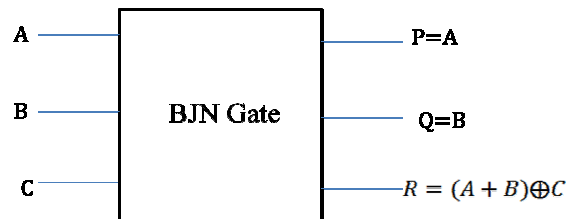

Fig 8: Block Diagram of BJN Gate

2.5 Peres Gate

The Peres Gate[12] incorporates the functions of both the CNOT and the Toffoli gate and is therefore useful for a large number of quantum operations. The Quantum Cost of Peres Gate is 4.
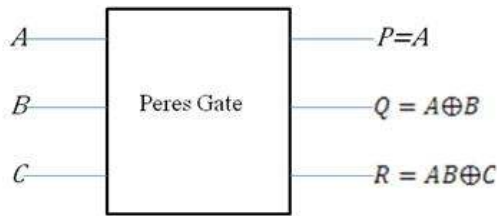
Fig 9: Block Diagram of Peres Gate

The Pauli-X gate[12] acts on a single qubit. It is the quantum equivalent of a NOT gate (with respect to the standard basis |0, |1, which privileges the Z-direction).

It equates to a rotation of the Bloch Sphere around the X-axis by p radians. It maps |0 to |1 and |1 to |0. It is represented by the Pauli matrix:
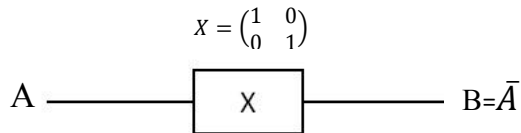
$$X = \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix}$$

Fig 10: Block Diagram of NOT Gate

3. RELATED WORKS

Moghimi[8] proposed a MOG gate which is capable of performing one bit parallel binary addition/subtraction and takes in four inputs A, B, Sel and C_{in} to produce the sum or the difference and the respective carry or borrow. The gate can be used in the generation of an ALU(Arithmetic Logic Unit) unit. The circuit diagram of the gate followed by its block diagram is shown below.
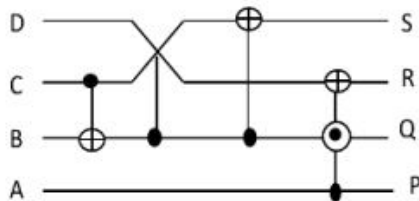

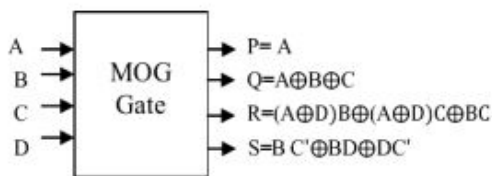**Fig 11: Circuit Diagram of Reversible MOG Gate**

Fig 12: Block Diagram of MOG Gate

The one and four bit implementation of the parallel adder/subtractor by Moghimi[8] is shown below.
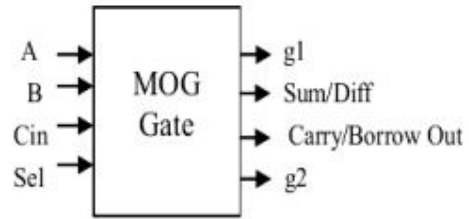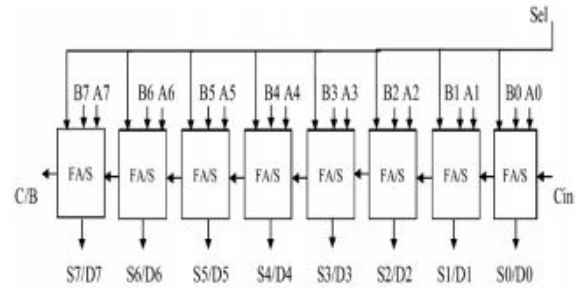

Fig 13: One bit Parallel Adder/Subtractor cell

Fig 14: 4 bit Parallel Adder/Subtractor using MOG Gate

Sel is used as the control line for performing addition or subtraction operation.

Rangaraju[7] proposed a design which was implemented using existing reversible gates. Three designs were proposed of which the most optimized one is shown below. The design consists of two Feynman gates and two Peres gates. The number of inputs is same as that of Moghimi[8] consisting of *Ctrl*, *A*,*B* and C_{in}.
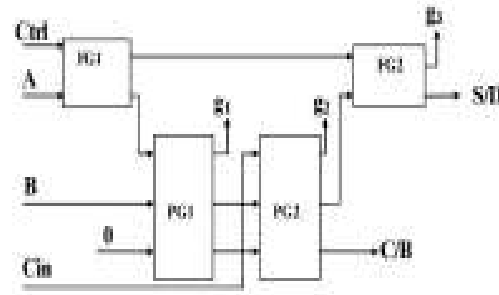

Fig 15: 1 bit Parallel Adder/Subtractor

The output is for Sum/Difference is denoted by S/D. Similarly Carry/Borrow is denoted by C/B.

4. PROPOSED METHOD

For implementing a parallel adder/subtractor, two Peres Gate and one Feynman Gate is used. The one bit implementation is shown below. Three inputs are supplied. "CTRL" acts as the control line which is used to control whether addition or subtraction operation is to be performed. "A" and "B" are inputs on which the operation is to be performed. The output for Sum/Difference, Carry/Borrow is denoted by "S/D" and "C/B" respectively.
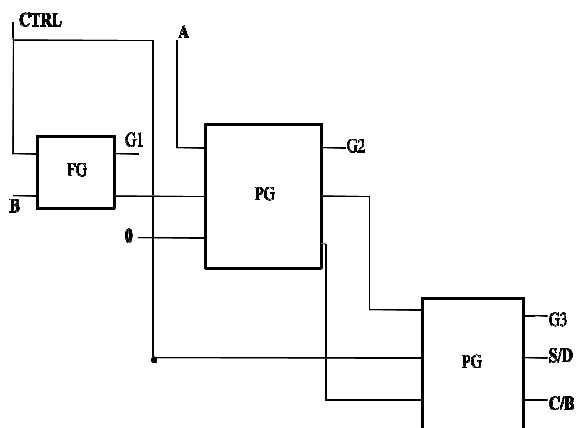
Fig 16: Implementation of 1 bit Parallel Adder/Subtractor

While implementing the Modulo circuit the following method was adopted. Consider two 4 bit numbers $A = A_3A_2A_1A_0$ and $B = B_3B_2B_1B_0$. The operation to be performed is $A \bmod B$. The two numbers is compared using a comparator circuit. The following three conditions are possible while comparing the two numbers.

(i) $A < B$
(ii) $A = B$
(iii) $A > B$

For condition (i) the output of the modulo circuit is A and the input at A is passed as the output. For condition (ii) the output of the modulo circuit is 0, as there can be no remainder on division. For condition (iii), B is subtracted from A and this process is repeated until either condition (i) or condition (ii) is achieved. The parallel adder/subtractor implemented above is used to perform the subtraction by setting the CTRL line to 1. The comparator circuit show below, proposed by Abbasalizadeh[11], is used for implementing the modulo circuit.
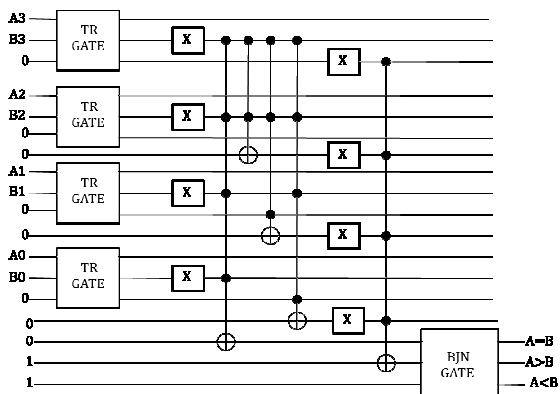

Fig 17: Comparator circuit

The output of the three comparison operations is obtained as the output of the BJN gate. The output from the line $A = B$ is fed into another BJN gate which produces a 0, as the output for the modulo circuit. For the output line $A > B$ in the comparator circuit, the value at A is obtained at the output by using a Toffoli gate. The BJN and Toffoli implementations are shown below.
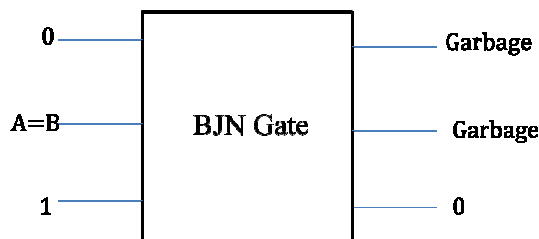
Fig 18: BJN Gate for A=B condition
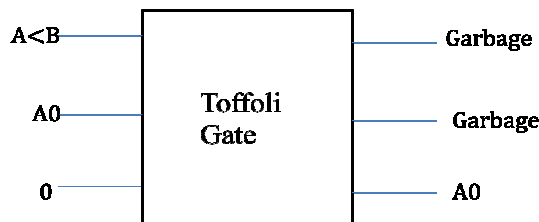
19: Toffoli Gate implementation for obtaining input bit as output

The output line $A > B$ is used to drive the parallel subtractor. For successive subtraction operations the output of each subtraction needs to be stored in a flip flop to be supplied as the input for the next operation. The D flip flop proposed by Basu[10] is used for this operation. The combined circuit for the modulo operation is shown below.
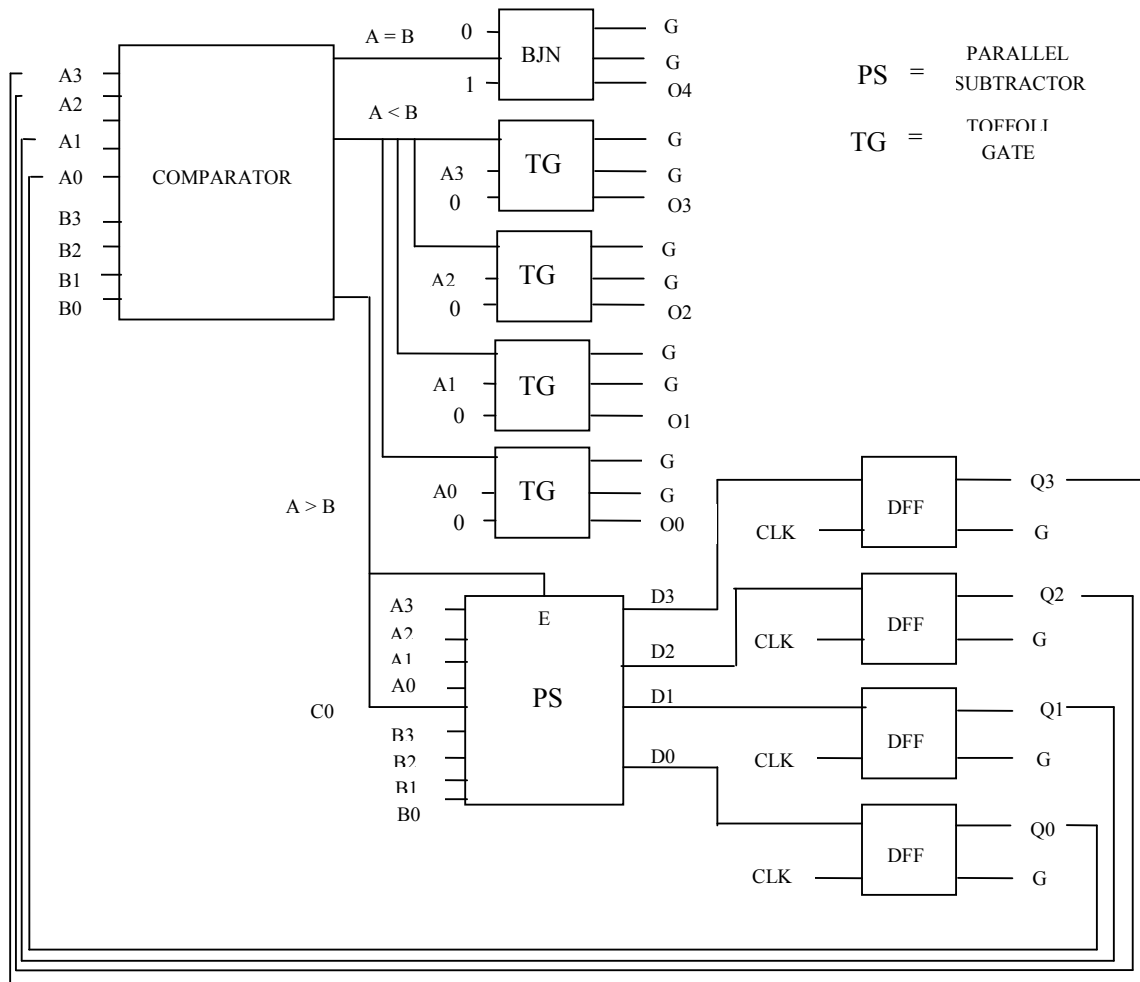
PS = PARALLEL SUBTRACTOR

TG = TOFFOLI GATE

Fig 20: Modulo Circuit implementation

5. RESULT ANALYSIS

The existing binary parallel adder/subtractor circuits [7][8] were compared with the proposed binary parallel adder/subtractor. The 4 bit implementations were compared on the basis of the number of gates required to build the quantum circuit, the quantum cost of the circuit and the number of Garbage outputs produced. The tables below show the comparison between the previous and proposed designs based on the above mentioned parameters.

Table 1: Comparison of Different Parallel Adder/Subtractor Circuits

Parameters of Comparison	Previous Methods		Proposed Method
Number of Gates	8	16	12
Quantum Cost	88	40	36

Number of Garbage O/P	16	12	12

The above tables validate that the proposed design is optimized under quantum cost and number of garbage outputs. Also, the design has been implemented using existing reversible gates unlike the design proposed by Moghimi[8].

The circuit used for implementing the modulo operation consists of a comparator module, a parallel subtractor module, 4 Toffoli gates, 4 D Flip-Flops and 1 BJN Gate. The quantum cost of the comparator module is 38[11].The 4 D Flip-Flops have a quantum cost of 20[10]. The parallel subtractor has a quantum cost of 36 and the combined quantum cost of the Toffoli Gates and the BJN Gate is 25. Hence the total quantum cost of the modulo circuit is 119. The total number of garbage outputs produced is 49 A tabular representation of the data is shown below.

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Table 2: Quantum Cost and the Number of Garbage outputs of each module

Module (M)	Quantum Cost	Number of Garbage O/P
M1: Comparator[11]	38	15
M2: D Flip Flops[10]	20	12
M3: Parallel Subtractor	36	12
M4: 4 Toffoli + 1 BJN	25	10

One aspect has to be kept in mind while implementing the circuit, i.e. there is no provision for feedback in reversible logic. But, in order to implement flip-flops, a feedback path is required. Moreover, the delay in reversible circuits is almost negligible. So, the feedback path with considerable delay is forcefully introduced in the circuit. Otherwise, the circuit without the delay will not be able to detect the feedback path and hence will give an erroneous output.[10]. The functionality of all the circuits has been verified, considering the delay factor in the feedback path, using Verilog and Modelsim.

6. CONCLUSION

The proposed reversible design of the binary parallel adder/subtractor is utilized for efficiently designing a circuit capable of performing modulo operation. Parallel Adder/Subtractor can be used in the generation of an ALU unit which is used for a large number of computations. By comparing the existing designs with the proposed one, it has been observed that the proposed design is less costly and also has a minimum number of garbage outputs. The proposed design is highly optimized. Thus, the reversible circuits incorporating this design are more cost effective. The presented modulo circuit is a novel one and can also be utilized in the implementation of an ALU. Since the modulo circuit has been implemented using the most cost effective components, it is also highly optimized.

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