

# A Novel High Input Impedance AC-Coupled Buffer

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#### ABSTRACT

Designing an AC-coupled buffer that works in the extremely low frequency range, a few Hertz, when the coupling capacitor is very small, a few pico-farads, forms a complex designing problem. In this article, a novel and simple scheme is proposed to realize such an AC-coupled buffer.

The proposed buffer shows extremely high input impedance at the low frequencies. This feature enables the proposed buffer to capture extremely low frequency signals which is coupled to it through a very small capacitor.

The main advantage of the proposed method is that, it can be implemented on a chip or by using general purpose discrete electronic components very easily.

The characteristics of the proposed buffer have been obtained and measured experimentally, analytically and, by using a computer aided design software.

## Keywords

AC-coupled buffer, impedance, frequency response, noise, generalized impedance converter

## 1. INTRODUCTION

The general structure of AC-coupled buffer is shown in Figure 1. The input signal, Vs, is coupled through a coupling capacitor, Cs, to the input of the buffer. In order to bias the input of the buffer, a DC path is also provided by

## resistor $R_b$ .

There are some applications that the input signal has extremely low frequency components and it is coupled through a very small capacitor to the input of the buffer. For example, in the non-contact electrocardiogram recording, the signal is coupled to the input of the buffer through an extremely small capacitor (a few pF), which is formed between the patient body and the electrode [1-5]. This limitation compels the designers to use a High input impedance buffer to capture the signal.

The design of an AC-coupled buffer in the extremely low frequency range forms a complicated challenge, when the coupling capacitor is very small (a few pF). In this case, the

size of  $R_b$  should be as high as possible (in order of T $\Omega$ ) to have a High input impedance buffer [1]. There are several ways to achieve this goal. One way is to utilize a resistor in the range of Tera-ohm. This solution could be implemented just by discrete components.

The bootstrap technique is a customary way to achieve a

high value of  $R_b$  virtually [6]. In the circuit which is shown in Figure 2 the Resistor  $R_{b1}$  is bootstrapped by  $C_b$ . The behavior of this circuit was analyzed in [6].



#### Figure 1: AC-coupled buffer

In the low frequency range, if a constant unity gain for buffer has been assumed, it is evident that the order of circuit is two. It is straightforward to show that the damping factor in this circuit is defined as equation (1).

$$\zeta = 0.5 \frac{R_{b1} + R_{b2}}{\sqrt{R_{b1}R_{b2}}} \sqrt{\frac{C_s}{C_b}}$$
(1)

As mentioned earlier the size of Cs is very small (a few pF), but on the other hand the value of Cb is chosen exteremely high in comparison with Cs to mitigate the destructive effect of bias resistors on the input impedance of the buffer, in the low frequency range. According to (1) and as shown in [6], the frequency response of the circuit shows a significant overshoot at the low frequencies. Therefore the circuit response is too oscillatory, furthermore it distorts the input signal significantly. Furthermore, in this method, the bias resistors and bootstrap capacitor are in the range of megaohm and micro-farad, therefore this technique is not suitable to implement on a chip.

In this article, based on Generalized Impedance Converter (GIC) circuit, a new high input impedance AC-coupled Buffer is introduced to overcome such limitations. The main advantage of the proposed method is that, it can be implemented on a chip or by using general purpose discrete electronic components very easily.





Figure 2: AC-coupled buffer by using bootstrap technique

## 2. A NOVEL HIGH INPUT IMPEDANCE AC-COUPLED BUFFER BASED ON GIC

The new proposed scheme to implement High input impedance AC coupled buffer has been presented in Figure 3. The input signal,  $V_s$ , is coupled to the proposed buffer

through the coupling capacitor,  $C_s$ . It is obvious that the

general structure of the proposed buffer is a well known GIC which was introduced and analyzed in [7]. The only difference is that the resistor R1 is replaced by two back to back series diodes, D1 and D2.

It is noteworthy to mention, that the diode based pseudoresistor is also used in some previous schemes along with bootstrap technique to realize high input impedance ACcoupled buffer [1]. But as mentioned earlier, the frequency response of the circuit shows a significant overshoot at the low frequencies due to the use of bootstrap technique. Furthermore the value of bootstrap capacitor is in the range of microfarad and it is impossible to implement such capacitor on a chip. In the proposed circuit the bootstrap technique is replaced by GIC circuit to implement high input impedance AC-coupled buffer. Therefore the proposed circuit could be realized on a single chip.

By assuming ideal Op-Amps, the voltage difference between two nodes, A and B, can be obtained as follow:

$$V_A - V_B = \frac{1}{K_r} V_A \quad (2a)$$
$$K_r = \frac{R_3 R_5}{R_2 R_4} \quad (2b)$$

In the proposed circuit, the value of  $K_r$  is selected extremely higher than unity. Therefore, According to equations (2a) and (2b), for a significant range of  $V_A$ , the voltage difference between two nodes, A and B, is very small.

According to the mentioned above, it is easy to show that two diodes act as a Resistor (R1). In order to show this fact and calculate R1, the resistance of each diode could be calculated by well known current-voltage ( $I_D$ - $V_D$ ) equation of a junction diode (3).

$$I_D = I_s \left( e^{\frac{V_D}{\eta V_T}} - 1 \right)$$
 (3)

Where  $I_s$ ,  $V_t$  and  $\eta$  are reverse saturation current, thermal voltage and ideality factor respectively.



Figure 3: novel proposed AC-coupled buffer

As mentioned earlier, in the proposed configuration the voltages through the diodes ( $V_{d1}$  and  $V_{d2}$ ) are very small, therefore the expression (3) can be simplified by the use of Taylor series and by using first order approximation. The relation between  $I_D$  and  $V_D$  of each diode can be written as equation (4a), by these simplifications. Therefore, it is clear that the equivalent resistor of each diode, Rd, is defined as equation (4b).

$$I_{D} = \frac{I_{S}}{\eta V_{T}} V_{D} \quad (4a)$$
$$R_{d} = \frac{V_{d}}{I_{d}} = \frac{\eta V_{T}}{I_{S}} \quad (4b)$$

According to equation (4b), the equivalent resistor of two diodes in the proposed buffer, R1, is defined as follow:

$$R_1 = 2R_d = 2\frac{\eta V_T}{I_s} \quad (4c)$$

Therefore the input impedance, Zin, of the proposed buffer has a real value in the low frequency range and, it can be written as equation (5), [7].



$$Z_{in} = R_{in} = \frac{R_3 R_5}{R_2 R_4} R_1 = K_r R_1 \quad (5)$$

It is noteworthy to mention that by using low leakage current diode, the value of R1 becomes very high (several Mega Ohm). Therefore In order to realize high input impedance buffer, the value of  $K_r$  should be chosen as high as possible.

As mentioned earlier the equation (5) is valid for the low frequency range and it has been obtained by assuming extremely high and constant open loop gain for operational buffers. The General expression for input impedance is as follow:

$$Z_{in}(s) = \frac{R_1}{1 - a(s)} \frac{M(s) - N(s)}{D(s)}$$
(6a)

a(s), M(s), N(s) and D(s) are defined as follow:

$$a(s) = \frac{A_0}{1 + \frac{s}{\omega_h}}$$
(6b)

$$M(s) = a(s) \cdot \begin{vmatrix} \frac{1+a(s)}{R_2} + \frac{1+a(s)}{R_3} & \frac{1}{R_3} \\ \frac{a(s)}{R_4} & \frac{1}{R_4} \end{vmatrix}$$
(6c)  
$$N(s) = a(s) \cdot \begin{vmatrix} \frac{1}{R_3} & -\frac{a(s)}{R_2} \\ \frac{1}{R_4} & \frac{1}{R_4} + \frac{1}{R_5} \end{vmatrix}$$
(6d)  
$$D(s) = \begin{vmatrix} \frac{1+a(s)}{R_2} + \frac{1+a(s)}{R_3} & -\frac{a(s)}{R_2} \\ \frac{a(s)}{R_4} & \frac{1}{R_4} + \frac{1}{R_5} \end{vmatrix}$$
(6e)

In the expression (6b), parameters  $A_0$  and  $\omega_b$  are the open-loop gain and the 3dB cutoff frequency of the Op-Amp respectively. The output to input voltage transfer Function of the proposed circuit,  $\frac{V_{out}(s)}{V_s(s)}$ , which is shown

in Figure 3, is as follow:

$$\frac{V_{out}(s)}{V_{s}(s)} = a(s)(1 - a(s)\frac{N(s)}{D(s)})\frac{Z_{in}(s)}{Z_{in}(s) + \frac{1}{C_{s}s}}$$
(7a)

In the low frequency range, expression (7a) can be simplified as follow:

$$\frac{V_{out}(s)}{V_{s}(s)} = (1 + \frac{R_{4}}{R_{5}}) \frac{R_{in}C_{s}s}{1 + R_{in}C_{s}s}$$
(7b)

In the equation (7b),  $R_{in}$  is defined by (5). The ideal goal is to have a flat output to input voltage transfer function in the low frequency range. It is apparent from equation (7b), this goal is reached by increasing the value of  $R_{in}$ . According to equation (5), the input impedance can be increased by increasing the value of  $R_1R_3R_5$  and/or by decreasing

 $R_2R_4$ . However, before deciding which resistors should be increased or decreased, the proposed network should be analyzed thoroughly. In the next section total output offset voltage and the noise of proposed circuit will be obtained. The obtained results then will be used to design the proposed buffer.

## 3. THE OUTPUT OFFSET VOLTAGE AND THE NOISE ANALYSIS

The total output offset voltage of the proposed buffer, which was presented in Figure 3, could be calculated by means of the model which is shown in Figure 4. In this model input offset voltage and input bias currents of an Op-Amp are modeled by independent voltage and current sources [8,9].



Figure 4: Op-Amp model for input bias current and offset voltage

The total output offset voltage of the proposed circuit has been obtained as follow:

$$V_{offset} = (1 + \frac{R_4}{R_5})K_r V_{os(a)} + (1 + \frac{R_5}{R_4})V_{os(b)} + (1 + \frac{R_4}{R_5})K_r R_2 (I_{B^-(a)} + I_{B^-(b)}) - R_5 I_{B^+(b)} + (1 + \frac{R_4}{R_5})K_r R_1 I_{B^+(a)}$$
(8)

The subscripts a and b in (8) is returned to Op-Amp a and b in Figure 3 respectively. According to expressions (5) and (8), in order to increase  $R_{in}$  and to keep output offset voltage low, R1 must be increased mainly in comparison with the other resistors of the proposed circuit. In this case, if the two Op-Amps are selected from same type, the first and last terms of equation (8) are dominant in comparison with the other terms. Therefore the equation (8) can be simplified as follow:



$$V_{offset} = (1 + \frac{R_4}{R_5}) \frac{R_3 R_5}{R_2 R_4} V_{os(a)} + (1 + \frac{R_4}{R_5}) \frac{R_1 R_3 R_5}{R_2 R_4} I_{B^+(a)}$$
(9)

It is noteworthy to mention that the Op-Amps should be selected from low input bias current types such as FET Op-Amps with the minimum offset voltage to reduce the total output offset voltage significantly. This output offset voltage can be eliminated by a simple high pass filter.

Another important feature of any amplifier is the noise performance. The Referred to Input (RTI) noise of an amplifier limits the minimum amplitude of a signal which can be detected and amplified by the amplifier. In order to perform noise analysis and calculate the RTI noise of the proposed circuit, the noise of resistors, diodes, and the voltage and the current noise of Op-Amps have been considered.

As mentioned earlier the value of R1 must be increased drastically to achieve a high input impedance buffer, but the spectral density of Johnson noise of a resistor is directly proportional to the value of the resistor [8]. Therefore, instead of using a resistor with high value, the resistor R1 is replaced by two series back to back diodes in the proposed circuit. As mentioned earlier the Op-Amps of the proposed buffer are selected from low input bias current types, such as FET input Op-Amps. Therefore the dc current of diodes are very small. This leads to the negligible shot noise and flicker noise.

Furthermore, if the other resistors have small values, typically lower than  $20K\Omega$ , the noise of these resistors is negligible and the noise analysis of the circuit becomes easier.

The complete circuit which is modeled the noise of Op-Amp is presented in Figure 5 [8,9]. The current noise in the two inputs of the Op-Amp are shown by two current sources,  $I_{p^+}$  and  $I_{p^-}$ . The voltage noise of Op-Amp is also shown

by a voltage source,  $V_n$ . This model has been employed to obtain the total output noise of the proposed circuit.



Figure 5: Op-Amp noise representation

By these assumptions the mean square of the total output noise of proposed Buffer could be written as equation (10a).

$$\overline{V_{on}^{2}} = \left[ (1 + \frac{R_{4}}{R_{5}})K_{r} \frac{1 + \tau s}{1 + \tau_{in}s} \right]^{2} \overline{V_{na}^{2}} + \left[ (1 + \frac{R_{4}}{R_{5}})K_{r} \frac{R_{1}}{1 + \tau_{in}s} \right]^{2} \overline{I_{na^{+}}^{2}} \\ + \left[ (1 + \frac{R_{4}}{R_{5}})K_{r} \frac{R_{2}}{1 + \tau_{in}s} \right]^{2} \overline{I_{na^{-}}^{2}} + \left[ (1 + \frac{R_{5}}{R_{4}})\frac{1 - \frac{R_{3}}{R_{2}}\tau s}{1 + \tau_{in}s} \right]^{2} \overline{V_{nb}^{2}} \\ + \left[ \frac{R_{5}}{1 + \tau_{in}s} \right]^{2} \overline{I_{nb^{+}}^{2}} + \left[ (1 + \frac{R_{4}}{R_{5}})K_{r} \frac{R_{2}}{1 + \tau_{in}s} \right]^{2} \overline{I_{nb^{-}}^{2}}$$
(10a)

Where  $\tau_{in}$  and  $\tau$  are defined as follows:

$$\tau = R_1 C_s \qquad (10b)$$
  
$$\tau_{in} = R_{in} C_s = K_r R_1 C_s \qquad (1)$$

The subscripts a and b in (10a) is returned to the Op-Amp a and b in Figure 3, respectively. If two OP-Amps are selected from same type, the expression (10a) could be simplified by neglecting the non-dominants terms. The simplified equation is as follow:

0c)

$$\overline{V_{on}^{2}} = \left[ (1 + \frac{R_{4}}{R_{5}}) K_{r} \frac{1 + \tau s}{1 + \tau_{in} s} \right]^{2} \overline{V_{na}^{2}} + \left[ (1 + \frac{R_{4}}{R_{5}}) K_{r} \frac{R_{1}}{1 + \tau_{in} s} \right]^{2} \overline{I_{na^{+}}^{2}}$$
(10d)

By using expression (10a) or (10d), it can be concluded that between two buffers which have same input impedance, the buffer which has greater R1 and lower  $K_r$ , shows lower total output noise and therefore lower RTI noise. This conclusion is verified in the next section experimentally and by using ORCAD simulator. It is noteworthy to mention that, the RTI noise could be obtained by dividing the Total output noise, (10a), by the gain of the amplifier which is defined by expression (7b).

#### 4. EXPERIMENTAL TEST

The network of Figure 3 is assembled by using AD795JK which is a FET Op-Amp. In the assembled circuit the diodes are 1N4148. The assembled circuit are also battery powered and the Op-Amps are supplied by  $\pm 12\nu$ . The coupling capacitor,  $C_s$ , is equal to 10pF. The PCB of the assembled circuit is single layer and it is also manufactured by the use of FR4 board.

The values of the other resistors are as follow:

$$R_3 = R_5 = 3 K \Omega$$

$$R_2 = R_4 = 133\Omega$$





Figure 6: output to input voltage transfer function

(Cs = 10pF)

Therefore the value of  $K_r$  is equal to 509. It is noteworthy

to mention that all resistors are in the range of several hundreds of ohm. The output to input voltage transfer function of the circuit,  $\frac{V_{out}}{V_s}$ , is measured experimentally

and also calculated by using ORCAD simulator and analytic method. It is noteworthy to mention that, in the experimental test, the input signal is a 1v pick-to-pick sinusoid signal. Furthermore, by the use of a Faraday shield the prototype is shielded to eliminate the power line interference. The results are shown in Figure 6. The obtained results show a flat response at the low frequency range, in spite of the extremely small coupling capacitor. Furthermore, the gain of the proposed buffer is close to unity in the pass band, as equation (7b) predicts.

The total output offset voltage of 120mV was also measured. The RTI noise is also obtained by the aid of ORCAD simulator and experimentally. In order to measure the RTI noise of the proposed buffer experimentally, the output signal of the proposed buffer is passed through a RC high-pass filter with 0.1Hz cutoff frequency. The output signal is then amplified by the use of non-inverting Op-Amp amplifier. The voltage gain of the non-inverting amplifier is 40dB and it has been implemented by using AD795JK Op-Amp. Finally the signal is passed through a simple RC Low-Pass filter to limit the bandwidth of the signal to 1 KHz. The signal is then sampled by the use of TDS2014C at 2.5KS/sec. The obtained results are shown in Figure 7.

In order to reduce the noise of the buffer, but maintain the gain, the value of R1 has been increased three times and, at the same time the value of  $K_r$  has also been reduced three times. Practically, each diode is replaced by three series diodes with the same direction. On the other hand, the value

of R5 is decreased three times and replaced by a  $1 \mbox{K} \Omega$  resistor.

By these measures, the input impedance of the buffer doesn't change and therefore the frequency response of the buffer remains as the previous case. The output to input voltage transfer function has been shown in Figure 8 and, it doesn't show any significant difference with the previous case (Figure 6).



Figure 7: Power spectral density of RTI noise (a) ORCAD simulation (b) Experimental measurement





Figure 8: The output to input voltage transfer function

The power spectral density of RTI noise of the new configuration is also shown in Figure 9. The comparison between these results and the previous case, Figure 7, shows significant reduction in RTI noise. In this case, the total output offset voltage of 80mV was also measured.

#### 5. CONCLUSION

In this article, a novel AC-coupled buffer has been introduced. The important advantage of the proposed circuit is that it could be implemented on a chip or by using discrete components very easily. The proposed buffer could be used at the extremely low frequency range, a few Hertz, and when the coupling capacitor is very small, a few pico-Farads.



Figure 9: Power spectral density of RTI noise (a) ORCAD simulation (b) Experimental measurement

#### 6. ACKNOWLEDGMENTS

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