Communications on Applied Electronics (CAE) – ISSN : 2394-4714
Foundation of Computer Science FCS, New York, USA
Volume 5 – No.5, July 2016 – www.caeaccess.org

FinFET Device Simulation and NAND Gate Implementation using DG FinFET

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ABSTRACT
In this paper it has been clarified that FinFET is a Fin Field effect transistor. It is promising substitute of CMOS in lower technology node. In this paper by making NAND Gate utilizing DG FinFET it is demonstrated that power utilization of IDDG FinFET is lesser than SDDG FinFET. At that point made an IDDG FinFET utilizing TCAD device and checked the impact of expanding the Fin width on the present qualities.

Keywords
Fin Field Effect Transistor(FinFET), Independently Driven Double Gate (IDDG), Simultaneously Driven Double Gate (SDDG)

1. INTRODUCTION
With progression in innovation and creation handle now it is conceivable to build the quantity of cells in a unit die die area with help of lower technology node. As CMOS is confronting bunches of difficulties with lower technology node like short channel impacts, process variety and because of these spillage increments and CMOS structure gets to be flimsy, so we are moving toward FinFET technology from technology node 22/24 nm and beneath. Multi gate structure is fundamentally of two sorts at Simultaneously Driven Double Gate (SDDG) and Independently Driven Double Gate (IDDG) [1]. As the name recommend in SDDG both gates are driven at the same time where as in IDDG both gates are driven autonomous to each other. In independently driven double gate device the limit voltage of one gate can adjust by giving the predisposition at another gate [2] [3].

In FinFET innovation we as a whole are having numerous choices and numerous advancements to utilize. There is double gate and triple gate FinFET additionally in the late patterns. Presently here I have utilized the double Gate FinFET technology and in that SDDG and IDDG NAND gate is made. With those both NAND gate the power prerequisite is ascertained and likewise it is picked that why IDDG is better contrast with SDDG at 22 nm technology node. Subsequent to understanding that data as IDDG power utilization is less one device is made up which is IDDG FinFET and in both the gate given diverse voltage and drive both the gate distinctively and after that by giving diverse Fin width what will be the impact of it on the FinFET qualities.

This paper is sorted out as in section 2 NAND gate setup of DG FinFET is clarified and its yield. In section 3 the IDDG FinFET device reenactment is clarified and its present qualities regarding change in Fin width. In section 4 the conclusion is there and finally references of this paper.

2. UNIVERSAL GATE USING DG FINFET

2.1 NAND Universal gate using SDDG FinFET
In this SDDG method of FinFET, i.e. simultaneously driven double gate FinFET both the gates are driven simultaneously. This arrangement is otherwise called Shorted gate FinFET implies as they are simultaneously driven so it additionally can be considered as shorted gate [4].

In the beneath figure the SDDG NAND is appeared.

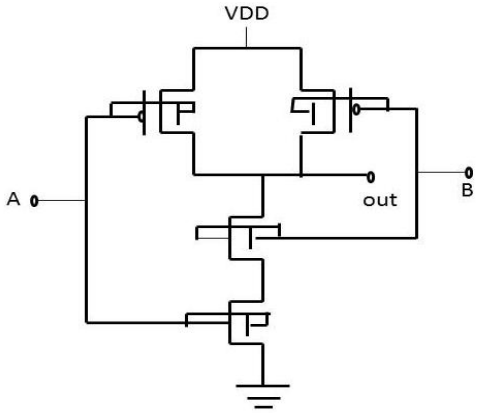

Fig. 2.1 NAND using SDDG FinFET

In the beneath figure the transient response of NAND gate utilizing custom wave viewer is appeared with 22 nm technology node.

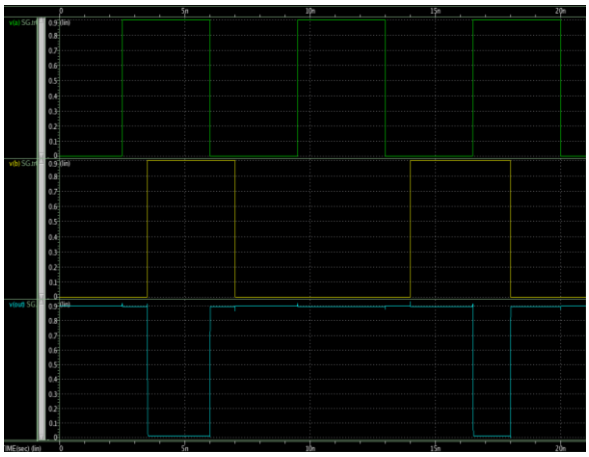

Fig. 2.2 NAND using SDDG FinFET Transient response

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2.2 NAND universal gate using IDDG FinFET

In this IDDG method of FinFET both the gates are independently driven. Free computerized signs are utilized as a part of this gate to drive the sign [4].

In the underneath figure IDDG NAND is appeared.

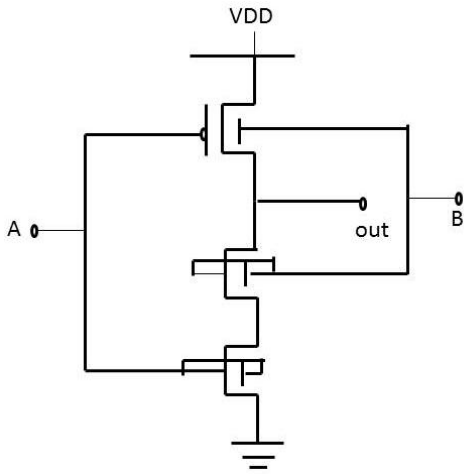

Fig. 2.3 NAND using IDDG FinFET

In underneath figure the transient reaction of IDDG FinFET utilizing NAND as a part of custom wave viewer is appeared with 16 nm technology node.

By making both the NAND gate circuits in Hspice apparatus when the power utilization is checked, the power utilization of SDDG mode is 1.1 times more than the force utilization in IDDG mode.

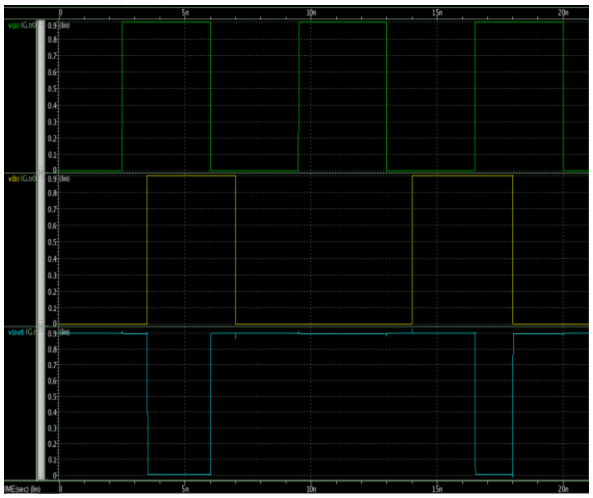

Fig. 2.4 NAND using IDDG FinFET Transient response

3. DEVICE SIMULATION

From above analysis it is demonstrated that power utilization of IDDG is lesser contrasted with SDDG FinFET. So from the assistance of TCAD apparatus one IDDG FinFET I have made in 2D design. It is appeared in underneath figure.

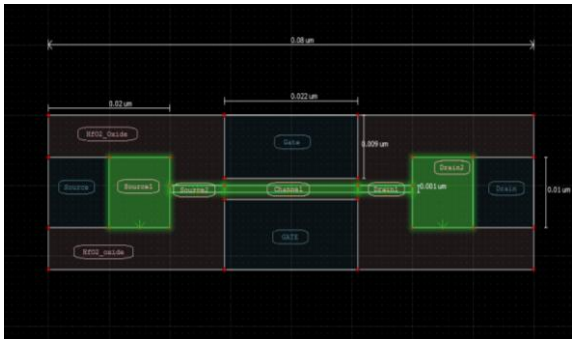

Fig. 3.1 22nm 2D IDDG FinFET

As appeared in above figure the IDDG FinFET is having Fin width of 1nm and gate length is 22 nm. By changing the Fin width from 1 nm to 4nm I have checked the yield qualities and in like manner it can be said that on the off chance that it builds the Id current likewise increments.

4. RESULTS

Table 1 Transient Analysis 22 nm FinFET

Mode	Transient Analysis		
	Power	***Rise Time***	***Fall Time***
SDDG	$1.17x10^{-7}$	$1.18x10^{-11}$	$1.75x10^{-11}$
IDDG	$1.06x10^{-7}$	$1.82x10^{-11}$	$1.69x10^{-11}$

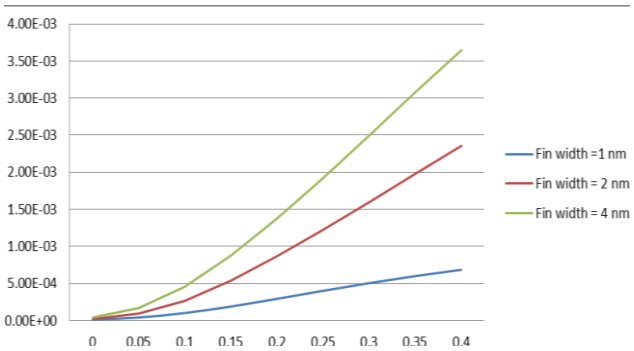

Fig. 4.1 Id vs Vg for IDDG FinFET

In the above graph the Drain current Versus Gate voltage graph for different width of Fin is shown in the above figure.

5. CONCLUSION

Work which has been done from the all inclusive gate NAND gate usage it can be said that power utilization is lesser in IDDG FinFET contrasted with SDDG FinFET. Rise time and fall time is likewise less of IDDG FinFET. Thus, when power is concern we ought to utilize IDDG FinFET as opposed to SDDG FinFET. At the point when Fin width builds the channel current likewise increments. So if Fin width increments there are odds of addition of power utilization.

6. REFERENCES

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