Communications on Applied Electronics (CAE) – ISSN : 2394-4714
Foundation of Computer Science FCS, New York, USA
Volume 5 – No.6, July 2016 – www.caeaccess.org

Insights of Performance Enhancement Techniques on FinFET-based SRAM Cells

Girish H.
Research Scholar,
J C BOSE Centre for
Research & Development,
Dept. of ECE, Cambridge
Institute of Technology,
K.R.Puram, Bangalore, India

Shashikumar D. R., PhD
Professor and HOD,
Dept. of Computer science Engg.
Cambridge Institute of Technology,
K.R.Puram, Bangalore, India

ABSTRACT
With the advancement in the energy efficient storage system, FinFET has already gained a pace in the area of computational memory management. However, after reviewing the research work focusing on FinFET based SRAM cells till date, we found that amount of research work towards enhancement of the design principle has not been much in number. Hence, we study some of the recently introduced research contribution towards enhancing the design performance of FinFET based SRAM cells and found that majority of the technique have both advantages and limitations too. We also highlights the significant research gap from the existing studies in order to assist the readers aware of the practicality of the research progress in this regards.

Keywords
FinFET, SRAM, Leakage Power, Energy Efficiency, CMOS, MOSFET

1. INTRODUCTION
With the modernization of the VLSI and need of superior grade storage system, FinFET SRAM has been evolved as a boon to offer 10nm size of transistor design [1]. The prime reason of this revolutionary technology is due to three dimensional design of the gate controls which is lowering its controlling dependencies from conventional drain and source terminal [2][3]. In conventional transistor design, inclusion of new components calls for short channel effect, which is completely mitigated by present design principle of FinFET [4]. Not only this, FinFET also addresses the problem of variation of arbitrary dopant as there is no channel doping mechanism in it. This phenomenon causes higher resistance from any form of potential errors or any other fluctuation caused from to process itself [5]. Along with this there are also less number of energy points as well as less number of points for product of delay and energy in FinFET circuits causing lowering of levels of supply voltage in comparison to planer CMOS design. Therefore, better stability in the voltage is achieved using FinFET. At the same time, the area of storage system like SRAM suffers from high allocation of cache memory in the chip area as well as it also suffers from maximum energy consumption of the chip power [6]. SRAM is used to perform three significant operation in a storage management i.e. standby, read, and write operation. SRAM is found better than DRAM with respect to volatility, speed, cost, density, reliability etc. The prime trade-offs in the design principle of the SRAM are i) speed vs leakage current, ii) read vs write stability, and iii) area vs yield. It is required that an SRAM cell should work faster and should dissipate less leakage power, which unfortunately is still an open end problem. The minimum voltage that a memory cell can use for performing reading operation is called as read voltage. Whereas the write voltage is just the opposite of it i.e. maximum voltage to perform write operation. Hence for better stability during read and write operation, it is required that read and write voltage should be kept minimum and driving strength of AC transistor should be make weaker and stronger during read and write operation respectively [7].

Another problem with existing SRAM is that it has shifted into the large scaled technologies in node design that consider smaller size with minimized level of voltage. This causes narrowing of the difference between the cut-off voltage and the supply voltage. Sometimes, the level of the voltage becomes highly unstable especially in the cache design in CPU where the system design calls for inclusion of transistors with higher reduced size in order to maintain large storage points. It is believed that voltage scaling causes bottlenecks in memory system and in order to address this problem, it is preferred to jointly study FinFET with SRAM. This integrated design principle offers a potential energy efficient feature in storage access design. We have also observed that there are lesser extent of studies that has focused on features of cache memories of SRAM cells. The prime difference between the conventional planar CMOS and FinFET is actually the fin, which is responsible for furnishing the channel for propagating the current in the switched on stage of the device. The gate surrounds the vertical fins on all the three sides in order to accomplish a superior control system over the channel. This control system automatically minimizes the short channel effect. The other significant attributes of FinFET are width of fin, height of fin, thickness, length of fin, and underlap of gate (i.e. distance between drain (or source) terminal to strip of gate). The incorporation of gate underlap assists in addressing the effect of current from source-to-drain, which further increase the robustness of FinFET devices to short channel effect. This paper reviews some of the techniques introduce most recently to enhance the design principles of FinFET based SRAM cells and discusses the research gap from the most recent literatures. Section II discusses about the essential of SRAM as well as FinFET design principle followed by discussion of existing techniques in Section III with respect to advantages and limitations of each techniques discussed in this section. Section IV briefs about the research gap after reviewing the existing system followed by Summary of the paper in Section V.

2. ESSENTIALS OF SRAM AND FINFET
As known RAM or Random Access Memory is one of the essential storage form in any forms of computing device. RAM is again classified into Static RAM (SRAM) and Dynamic RAM (DRAM). SRAM uses 6 transistors of cell structure to store a bit of data. It is characterized by beneficial factors e.g.

Communications on Applied Electronics (CAE) – ISSN : 2394-4714
Foundation of Computer Science FCS, New York, USA
Volume 5 – No.6, July 2016 – www.caeaccess.org

faster access, less power utilization although it is quite expensive to design [8]. Normally, flip-flop circuit is used for developing SRAM cells and is found to usually used with Field Effect Transistor (FET or unipolar transistor) [9]. The prime purpose of FET is to channelize the transmission from source to drain. There are three types of terminals in FET i.e. source, drain, and gate, which can be seen on any cross section of MOSFET as shown below:

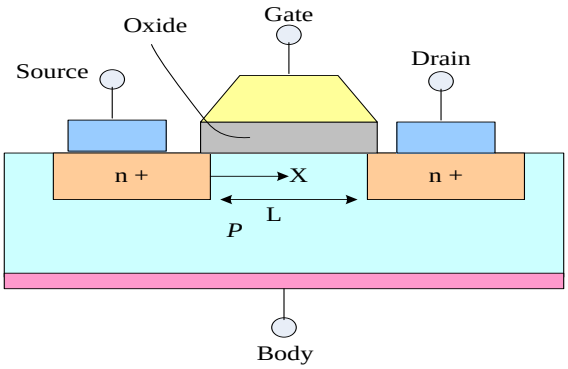
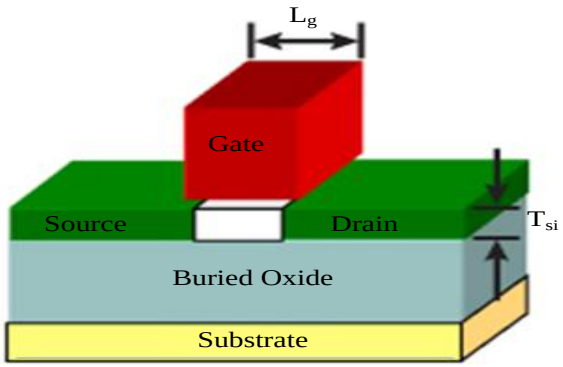
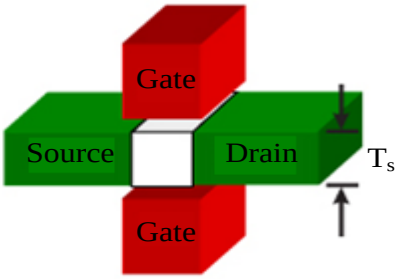


Figure 1. MOSFET Cross Section

As SRAM is majorly implemented with FinFET, so it is essential to brief about evolution and operations of FinFET that has evolved during 1990 by DARPA. A novel structure for a unique transistor was presented by Dr. Chenming Hu in order to minimize leakage current. The research towards FinFET was then taken over by group of researchers in Berkley who recommended use of MOSFET of thin body to minimize leakage. Fig.2 shows the original structure of FinFET.



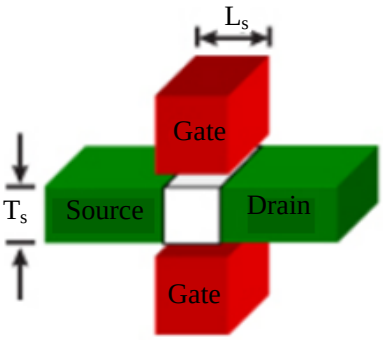
(a) Ultra-Thin Body



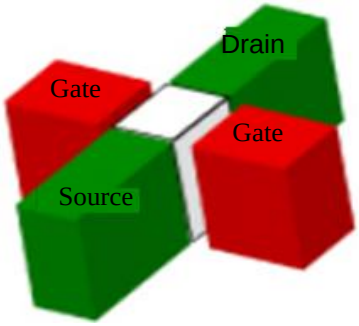
(b) Double Gate

Figure 2 Evolution of FinFET from MOSFET

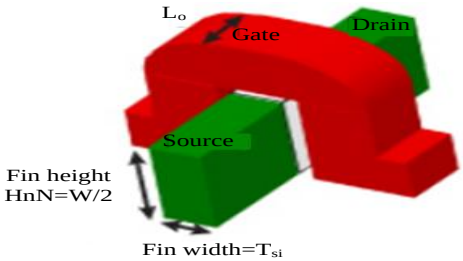
The evolved structure assists in minimizing the leakage current by changing the orientation of the original double gate structure (Fig.2(b)). This phenomenon allows auto aligning of the gate electrodes by conventional lithography methods which is almost equivalent to planar structure of FET (Fig.3(a))



(a) Planer-double Gate FET



(b) FET with 90% rotation



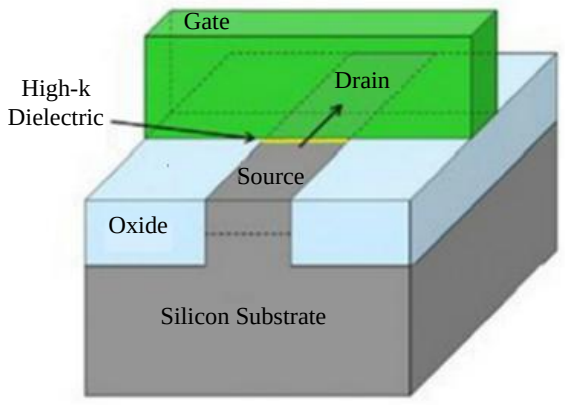
(c) FinFET

Figure 3 Evolution of FinFET

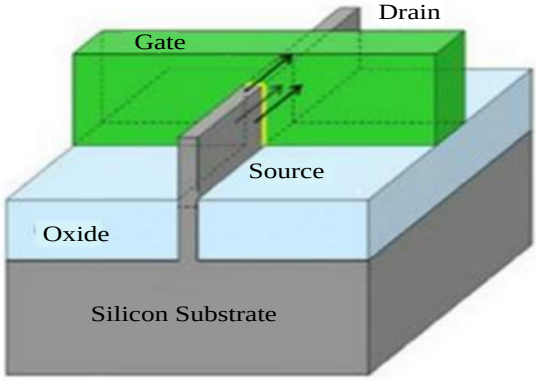
The FinFET design at present time is highly three dimensional and offers all possible way to minimize the leakage of power from its body during the off state of FinFET device. It was also believed that scalability of the FinFET can be maintained by scaling the channel thickness.

2.1 Aim of FinFET

The general aim of adoption of FinFET is to mainly ensure the reduction of leakage current to maximum degree although the processing cost of its three dimensional structure can slightly go up to 5% as compared to planer structure. The FinFET ensure 37% increment in speed along with 90% of minimization of leakage current.



(a) Conventional Planar Transistor



(b) 3D Tri-Gate Transistor (FinFET)

Figure 4 Difference between Conventional Planar and 3D FinFET

Usage of FinFET allows the transistor designer to operate it quite faster using equivalent quantity of power. Another aim of FinFET is to offer superior processing of Integrated Circuits. The generalized aim of FinFET are stated as following:

- To offer highly minimal power consumption in higher level of integration.
- Due to usage of lower cut-off voltage, FinFET is dependent on only lower operating voltage.
- FinFET offers a size upto 20nm as maximum.
- 90% reduction in static leakage power.
- The operating speed of FinFET is 30% faster compared to other types.

2.2 Tool of FinFET

At present there are various tools which offers digital designing of FinFET with better accuracy e.g. RC (Resistance Capacitance) Extraction Tools [10], SPICE Simulation Tools [11], TCAD Tools [12], and Physical verification tools [13]. The RC (Resistance Capacitance) Extraction Tools is basically used for investigating the effect of parasitic effects in the form of resistance and capacitance. One of such product is StarRC from Synopsys [10]. SPICE is one of the most frequently used simulation tool in research by various names e.g. HSpice, FineSim Spice, CustomSim Spice, FastSPICE etc. It possess an extensive library of transistors and circuitry design. TCAD tools are basically used for optimization purpose and is used to study multiple effects by simulation. Physical verification tools are basically used for validating the industrial design of FinFET using a ruleset. Such rule sets are used for authenticating the effectiveness of logic correctness and design rule checks.

2.3 Performance Parameters

At present, it is found that existing research work towards FinFET SRAM uses three performance parameters e.g. Leakage power drainage, Static Noise Margin, and Propagation Delay. From majority of the study the leakage power consumption is found within a range of 27-70^{o}C for standard 6 transistors configuration. The static noise margin can be defined as exact amount of voltage of DC noise in order to perform flipping operation of respective states of SRAM cells of specific configurations. The last parameter called as propagation delay is mainly associated with reading operation of FinFET and is represented as time that is needed to voltage difference of specific value (200mV) between BL and BLB.

The next section discusses about the existing techniques where various design principles for enhancing FinFET SRAM has been discussed.

3. EXISTING TECHNIQUES

This section discusses about the most recently presented technique for improving the design aspect of FinFET SRAM operation in research area. The conceptual discussion of FinFET SRAM has bulk of research papers and there are some survey papers [14] that has already covered up the discussion of techniques till 2013. However, none of the existing review papers has discussed the comparative analysis of existing techniques with respect to beneficial features and limiting features of existing techniques. Hence, this section of the paper will discuss the existing techniques for enhancing the design of FinFET SRAM published between 2013-2016.

The design aspects of the SRAM could be significantly improve by focusing on the nanometer area which could be populated with various alternative devices of Field Effect Transistors i.e. FET. The recent review performed by Parimaladevi et al. [15] have discussed about the performance factor of the SRAM and has theoretically discussed multiple solutions. The study assists to understand two facts i.e. i) there are better scope of FET in SRAM for design improvement and ii) the design of FET itself can be hybridized to attain better objectives. Similar review was also carried out by Bhattacharya and Jha [16]. Discussion on design challenges on FinFET was carried out by Burnett et al. [17]. The most recent study of Zhang et al. [18] [19] have emphasized on low powered applications with FinFET technologies of 7/8 nm. The prototype designed by the author was used to gauge the SRAM with 6 transistors. The study outcome was evaluated with respect to current and voltage. Study towards significance of FinFET on the design improvement was also recently carried out by Lee [20]. The authors presents elaborated discussion towards bulk FinFET and compared its performance over with another type of the FinFET i.e. SOI FinFET. The evaluation was carried out over 14 nm of node and was tested with respect to current-voltage charecteristics. The study has also investigated about the trends of heat dissipation from the 14nm node to find the temperature reduction capability of 325 K. Study in similar direction was also carried out by Song et al. [21] most recent in 2016. The author have introduced the similar design principle with 10nM of node with FinFET on SRAM with 128 Mb capacity.

Ansari et al. [22] have presented an elaborated study of design improvement of SRAM cells with 7 transistors. The author has considered a simulation-based study with HSPICE using multiple number of transistor (20, 16, 14, 10, 7 nm). The outcome of the presented simulation study was found to possess better write speed as well as enhanced stability. The mean static power was also found to be reduced by approximately 57% with existing design of 5T SRAM. A trend of using multiple numbers of transistors involvement was investigated by various researchers. The work carried out by Dani et al. [23] have discussed the charecteristics of 6T SRAM design using FinFET with respect to standby mode, read / write mode, etc. The simulation study outcome was evaluated with respect to power and delay mainly for both read / write operation. Similar trend of study on 6T SRAM was also carried out by Gupta and Roy [24]. Same year (i.e. 2015), Kushwah and Akashe [25] have presented a technique of enhancing the stability of noise margin using SRAM cells with 6 transistors. The study outcome shows better feasibility of stability enhancement during read operation and minimizing the voltage reduction and leakage current. Hence, it can be seen that there are many researchers who choose to implement in SRAM cells with 6 transistors. However, usage of 6 transistors cannot be used to accomplish near-cut-off voltage which is quite important for devices with restricted energy. This problem was addressed by Park et al. [26] where a unique buffer for reading operation was introduced with near cut-off voltage. The outcome shows better write capability with stabilized device operation. Similar direction of the study using SRAM cells with 6 transistors and 22 nm FinFET device was also investigated by Manju and Kumar [27]. The author have considers access time variation between read and write operation in order to maximize it.

Farkhani et al. [28] have presented a new SRAM design with cell size of 65nm for incorporating new methods in read / write operations. The technique uses non-positive voltage for enhancing the write characteristics of SRAM cells. The complete design evaluation was done for SRAM cells with 10 transistors. The simulation outcome of the study was found to possess 82% enhancement to write operation in contrast to conventional SRAM cells with 8 transistor.

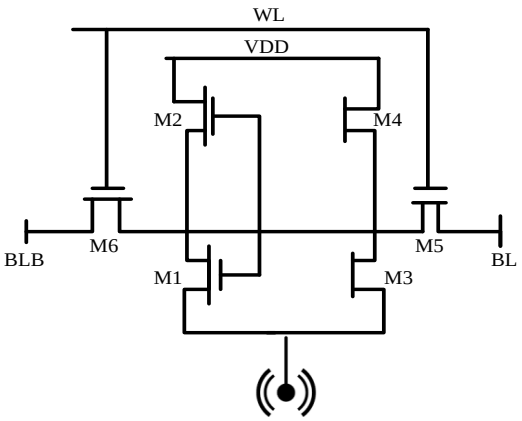


Figure 5. Design of 6T SRAM by Dani et al. [L7]

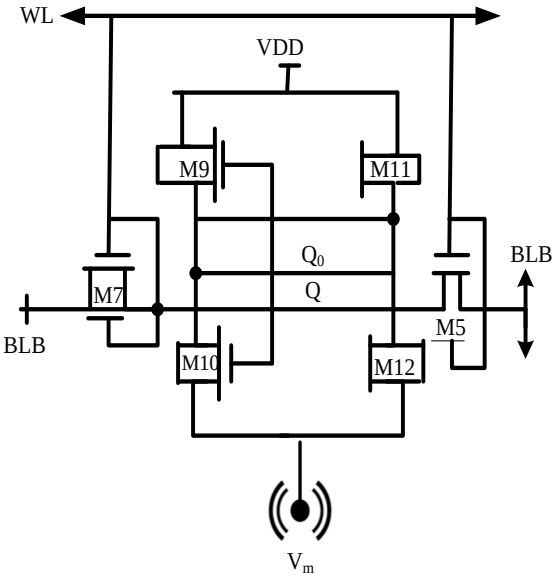


Figure 6 Design of 6T SRAM by Kushwah [L10]

Shafaei et al. [29] have presented a unique technique to improving performance of FinFET devices. The authors have built a 6T and 8T SRAM cells with 7nm of FinFET device. The overall study objective was to attain the energy efficient cache memory on FinFET device. Zeinali et al. [30] have presented a study using SRAM cells of 9 transistors with 14 nm FinFET device. The study outcome shows minimization of leakage power by 20% and enhancement of memory access time by 30%. Pal et al. [31] have introduced a double dielectric for enhancing the electrostatic integrity of FinFET in SRAM. Ghai et al. [32] have presented a study that compares the multiple significant parameters for FinFET with respect to analog design. Kerber et al. [33] have developed a double gated FinFET to checks its influence due to strained effects of silicon on static memory. The study outcome shows enhancement in read / write stability in comparison to unstrained FinFET. Villacorta et al. [34] have focused on reliability of SRAM using statistical approach. The summary of above discussion is tabulated below:

Table 1 Summary of Techniques for Design Enhancement of FinFET SRAM

Authors	Technique	Advantage	Limitation
Parimaladevi et al. [15]	Theoretical study of SRAM	Simple description of FET technologies	Doesn't specifically highlight the best solution.
Zhang et al. [18][19]	SRAM with 6T, FinFET	Saving of 20% of cell area	Study lacks benchmarking
Lee [20]	14nm, Bulk & SOI FinFET	325K of temperature reduction	-No Benchmarking
Song et al. [21]	10nm, FinFET SRAM, 128 bit	Better power gain	-No Benchmarking
Ansari et al. [22]	7T-SRAM	Highly stable, 57% of reduced power consumption	-No Design optimization
Dani et al. [23] Gupta and Roy [24], Kushwah and Akashe [25]	6T SRAM, FinFET	-8.9% of improvement of static noise margin in 16nm cell -better delay and energy performance	-less extensive analysis of outcomes to prove system stability on dynamic load.
Park et al. [26], Manju and Kumar [27]	Buffer with read operation, 6T SRAM, 22 nm FinFET	Better write ability, stabilized operation.	-Computational Complexity is not evaluated.
Farkhani et al. [28]	10T SRAM,	-82% improvement of existing write operation. -Supply voltage reduced to 24%. -33% minimization of leakage power	-Less Effective benchmarking
Shafaei et al. [29]	6T, 8T SRAM with 7nm FinFET, cross layer	-memory efficient memory	-No variability analysis considered. -outcome validation not done.
Zeinali et al. [30]	9T SRAM, 14 nm FinFET	-30% improvement of existing read operation. -20% minimization of leakage power	-Less Effective benchmarking
Pal et al. [31]	Double dielectric, 22nn FinFET	-reduction of 56% and 17% of read & write access time	-Computational Complexity is not evaluated.
Ghai et al. [32]	Comparison of FinFET parameters	-outcomes applicable in analog circuit design	-Computational Complexity is not evaluated. -No Benchmarking
Kerber et al. [33]	Investigation on Strained Effect on silicon	10-20% enhancement of read-write stability.	-Computational Complexity is not evaluated. -No Benchmarking
Villacorta et al. [34]	Hardening of SRAM FinFET	Enhance critical charge	-Less Effective benchmarking

4. RESEARCH GAP

This section discusses about the research gap of the existing techniques to improvise the design aspects of SRAM cells and FinFET technologies.

- *Less Extent of Novelty*: We have observed that studies pertaining to improve the SRAM cell performance is done majorly either by changing the number of transistors or by using various size of FinFET device, which becomes an impediment towards any future scope of optimization.
- *Less number of computational Modelling*: Majority of the existing mechanism chooses to use either experimental approach or by using hardware-based simulation environment for SRAM and FinFET. Experimental approaches give highly reliable outcomes but none of the studies done till date have actually checked for computational complexity, which makes the approach less applicable in real-time and big-scale commercial usage. Hardware-based approach uses a specific simulation environment which narrows down the scope of computational capability in this.
- *Less Studies toward Optimization*: There is a need to develop a computational optimization model in order to enhance the design performance of SRAM FinFET as well as to address the problems of fault tolerance too. There is a need of mathematical optimization principle supported by probability theory for giving better edge to the upgradation of design principles of SRAM based FinFET. There is also a need to focus on the variability

factor which has received less attention till date in this field except for few number of studies.

- *Lack of Benchmarked Research Work*: Till date, there are approximately 378 research papers (297 conference and 79 journals) dedicated for SRAM FinFET till date, which is extremely less in number of research work. Even in this less extent of work, the existing studies have witness various differentials in terms of approaches. We have observed that majority of the outcome of the studies are not found to be benchmarked with some standards which makes it quite hard to make out the best approaches or technique till date.

5. CONCLUSION

The topic or problems related to FinFET SRAM is not new as there are approximately 738 Journals focusing on the problems related to SRAM published during the year 2010-2016 in IEEE Xplore and there are approximately 378 Journals focusing on the problems related to FinFET published during the year 2010-2016 in IEEE Xplore. There are many problems in this topic, but it is required to choose such a problem, where we don't have much research work. Hence, some unique problem, which are found to be less addressed in IEEE transaction papers are: i) Ignorance towards Fault Tolerance: It is discussed on many papers that gate tunneling and threshold current during read/write process are highly influenced by static leakage current in FinFET SRAM. Usage of computational model of optimization is also less found in literatures. ii) Vague implication of optimization: Majority of the existing literatures just perform minor improvement of performance parameters and claimed it as optimization. Whereas in real-sense, none of the paper related to FinFET SRAM is found actually implement optimization modelling. However, there are few papers e.g. Wang [35], Lu [36], and Kashfi [37]. A closer look into all the IEEE papers on FinFET SRAM will show that their approach is like fine-tuning the technology in order to ensure better customization of transistor charecteristics. However, none of the techniques implemented till date in this can be never considered to be sufficient enough as a transistor will always need to design requirements with respect to system, circuits, and corresponding application. It was because; enough computational modelling is missing from literatures. Moreover, now we have more problems (but specific) to address i.e. fault tolerance, energy efficiency, and high level optimization, for which we do not have any transaction papers to claim so in FinFET SRAM published between 2010-2016. Therefore, our future direction of the work will be to develop a computational model for high level of design optimization of FinFET SRAM. Following are the objectives to be fulfilled i.e. i) To develop a simple and cost effective fault-tolerant model that can significantly optimize stochastically the design performance of FinFET SRAM, ii) To apply a predictive approach for further optimizing design state of FinFET SRAM for enhanced throughput, and iii) To further perform high-level optimization for better stability and energy effectiveness (dynamic).

6. REFERENCES

[1] Chen, Emerging Nanoelectronic Devices, John Wiley & Sons, 2015

[2] R. Reis, Y. Cao, G. Wirth, Circuit Design for Reliability, Springer, 08-Nov-2014

[3] N. Kaushik, B.K. Kaushik, D. Kaur, M.K. Majumder, "Independent Gate SRAM based on Asymmetric gate to Source / Drain Overlap-Underlap Device FinFET", *Springer- Progress in VLSI Design and Test: 16th International Symposium on VSLI Design and Test*, 2012

[4] W. Han, Z. M. Wang, 'Toward Quantum FinFET', Springer Science & Business Media, 2013

[5] C. Shin, 'Variation-Aware Advanced CMOS Devices and SRAM', Springer, 2016

[6] B. Prince, 'Vertical 3D Memory Technologies', John Wiley & Sons, Aug-2014

[7] K. Ishibashi, K. Osada, 'Low Power and Reliable SRAM Memory Cell and Array Design', Springer Science & Business Media, 2011

[8] G. Nicolescu, I. O'Connor, C. Piguet, 'Design Technology for Heterogeneous Embedded Systems', Springer Science & Business Media, 2012

[9] D. Chattopadhyay, Electronics (fundamentals And Applications), New Age International, 2006

[10] http://www.synopsys.com/Tools/Implementation/SignOff/Pages/StarRC-ds.aspx

[11] http://www.ti.com/tool/tina-ti

[12] http://www.synopsys.com/tools/tcad/Pages/default.aspx

[13] https://www.mentor.com/products/ic_nanometer_design/verification-signoff/physical-verification/

[14] M. Bayoumi, A. Dutta, "FinFET based SRAM Design: A Survey on Device, Circuit, and Technology Issues", *IEEE International Conference on Electronics, Circuits and Systems*, pp/387-390, 2014

[15] M.Parimaladevia, D.Sharmilab, L.Kowsikaa, "A Survey on the Performance Analysis of 6t Sram Cell Using Novel Devices", *South Asian Journal of Engineering and Technology*, Vol.2, No.18, pp.71–77, 2016

[16] D. Bhattacharya and N. K. Jha, "FinFETs: From Devices to Architectures", *Hindawi Publishing Corporation*, Advances in Electronics, 2014

[17] D. Burnett, S. Parihar, H. Ramamurthy, S. Balasubramanian, "FinFET SRAM Design Challenges", *IEEE International Conference on IC Design and Technologies*, pp.1-4, 2014

[18] X. Zhang, D. Connelly, P. Zheng, H. Takeuchi, "Analysis of 7/8-nm Bulk-Si FinFET Technologies for 6T-SRAM Scaling", *IEEE Transactions On Electron Devices*, vol. 63, no. 4, april 2016

[19] X. Zhang, "Simulation-based Study of Super-steep Retrograde Doped Bulk FinFET Technology and 6T-SRAM Yield", Doctorial Thesis on University of California at Berkeley, 2016

[20] J.H. Lee, "FinFETs: Design at 14 nm Node and Key Characteristics", *Springer Journal of Nano Devices and Circuit Techniques for Low-Energy Applications and Energy Harvesting*, 2016

[21] T. Song, W. Rim, S. Park, Y. Kim, "A 10nm FinFET 128Mb SRAM with Assist Adjustment System for Power, Performance, and Area Optimization", *IEEE International Solid-State Circuits Conference*, 2016

[22] M. Ansari, H. A. Kusha, B. Ebrahimi, Z. Navabi, "A near-threshold 7T SRAM cell with high write and read margins and low write time for sub-20 nm FinFET technologies", *Elsevier Journal of INTEGRATION, the VLSI journal*, vol.50, pp.91–106, 2015

[23] L. M. Dani, G. Singh, M. Kaur, "FinFET based 6T SRAM Cell for Nanoscaled Technologies", *International Journal of Computer Applications*, Vol.127, No.13, October 2015

[24] S. K. Gupta and K. Roy, "Low Power Robust FinFET-Based SRAM Design in Scaled Technologies", *Springer Journal of Circuit Design for Reliability*, 2015

[25] R. S. Kushwah and S. Akashe, "FinFET-based 6T SRAM cell design: analysis of performance metric, process variation and temperature effect", *InderScience International Journal of Signal and Imaging Systems Engineering*, Vol. 8, No. 6, 2015

[26] J. Park, Y. Yang, H. Jeong, S. C. Song, J. Wang, "Design of a 22-nm FinFET-Based SRAM With Read Buffer for Near-Threshold Voltage Operation", *IEEE Transactions On Electron Devices*, vol. 62, no. 6, June 2015

[27] I. Manju, A. S. Kumar, "A 22 nm FinFET based 6T-SRAM cell design with scaled supply voltage for increased read access time", *Springer Analog Integration Circular of Signal Process*, 2015

[28] H. Farkhani, A. Peiravi, F. Moradi, "A new write assist technique for SRAM design in 65 nm CMOS technology", *Elsevier- Integration, the VLSI journal*, vol.50, pp.16–27, 2015

[29] A. Shafaei, S. Chen, Y.Wang and M. Pedram, "A Cross-Layer Framework for Designing and Optimizing Deeply-Scaled FinFET-Based Cache Memories", *Journal of Low Power Electronics and Applications*, vol.5, pp.165-182, 2015

[30] B. Zeinali, J. K. Madsen, P. Raghavan, F. Moradi, "Sub-threshold SRAM Design in 14 nm FinFET Technology with Improved Access Time and Leakage Power", *IEEE Computer Society Annual Symposium on VLSI*, 2015

[31] P. K. Pal, B. K. Kaushik, S. Dasgupta, "Design Metrics Improvement for SRAMs Using Symmetric Dual-k Spacer (SymD-k) FinFETs", *IEEE Transactions On Electron Devices*, vol. 61, no. 4, April 2014

[32] D. Ghai, S. P. Mohanty, and G. Thakral, "Comparative Analysis of Double Gate FinFET Configurations for Analog Circuit Design", *IEEE International Midwest Symposium on Circuits and Systems*, pp.809-812, 2013

[33] P. Kerber, R. Kanj, and R. V. Joshi, "Strained SOI FINFET SRAM Design", *IEEE Electron Device Letters*, vol. 34, no. 7, July 2013

[34] H. Villacorta, V. Champac, S. Bota, J. Segura, "FinFET SRAM hardening through design and technology parameters considering process variations", *IEEE European Conference on radiation and Its Effects on Components and Systems*, pp.1-7, 2013

[35] Wang, Modeling leakage power reduction in VLSI as optimization problems, Springer, 2007

[36] Lu, Layout Optimization in VLSI Design, 2001

[37] Kashfi, Multi-objective optimization techniques for VLSI circuits, 2011

7. AUTHOR PROFILE

Girish H
He received his B.E in ECE from Kuvempu University, Karnataka, India and M Tech from Visveswaraya Technological University (VTU), Belgaum, India. He is pursuing PhD in VTU. His area of interest is VLSI. He is currently working as Associate Professor in Department of Electronics and Communication, Cambridge Institute of technology, Bangalore-36, India.

Dr. Shashikumar D R
He received his B.E in ECE from Mysore University (MU), Karnataka, India & M.E from Bangalore University (BU), Karnataka, India. He received his PhD degree from Fakir Mohan (FM) University, Balasore, Orissa. His area of interest is VLSI, image Processing. He is currently working as Professor and Head of the Department of Computer Science Engineering, Cambridge Institute of technology, Bangalore-36, India. He has published more than 20 International journals and 20 National journals. Currently, he is guiding 6 PhD scholars.