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Design of Reversible Logic based Basic Combinational Circuits

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ABSTRACT
With advances in VLSI technology, we are able to integrate more and more devices on single unit area to build more and more low power portable applications. As device size decreasing power dissipation becoming major concern for the design. In order to build low power systems there is a need for new technology which adapts logic which conserves energy and dissipates no power. Such upcoming technologies are quantum computing, quantum cellular automata, DNA computing, Optical computing and nano technologies. we have reversible circuits which dissipates no power or with zero internal power dissipation.. So there is a need for building combinational and sequential reversible circuits so that future computer can be replaced.. Attempt is made in this paper to build basic combinational logic circuits using reversible gates to minimize quantum cost, garbage outputs, ancilla inputs and gates. Results are verified using Xilinx14.2 tool with Spartan3 FPGA kit**.**

Keywords
Reversible, Garbage output, Quantum cost, Ancilla input

1. INTRODUCTION
As the technology is advancing we are building more and more portable devices by integrating more number of devices. Therefore energy dissipation is becoming key issue to be solved. R. Landauer in the year 1960 has demonstrated that energy dissipation due to information loss is high when circuits are constructed using irreversible logic. According to Landauers principle, the loss of one bit of information lost, will dissipate kT*ln (2) joules of energy where, k is the Boltzmanns constant and k=1.38x10 -23 J/K, T is the absolute temperature in Kelvin [1]. The basic combinational circuits dissipate heat energy for every bit of information lost during the operation. This is because according to second law of thermodynamics, information once lost cannot be recovered by any methods. In 1973, Bennett, showed that in order to avoid kTln2 joules of energy dissipation in a circuit it must be built from reversible circuits [2]. According to Moores law the numbers of transistors will double every 18 months. Thus energy conservative devices are in need today. Reversible circuits are those circuits that do not lose information. The most important application of reversible logic lies in quantum computers [3]. A quantum computer will be viewed as a quantum network composed of quantum logic gates , with applications in various research areas like Low Power CMOS design, quantum computing, nanotechnology and DNA computing. Reversible computation in a system can be performed only when the system comprises of reversible gates. A gate is said to be reversible if the input vector can be uniquely recovered from the output vector and there is a one-to-one mapping between its input and output assignments [4-5].The main challenges of designing reversible circuits are to reduce the number of gates, garbage outputs, constant inputs and quantum cost.

1.1 Basic Definitions related to reversible logic

Reversible logic gate
Reversible Gates are circuits in which number of outputs is equal to the number of inputs and there is a one to one correspondence between the vector of inputs and outputs [7]. It not only helps us to determine the outputs from the inputs but also helps us to uniquely recover the inputs from the outputs

Constant inputs:
This refers to the number of inputs that are to be maintaining constant at either 0 or 1 in order to synthesize the given logical function [8].

Garbage outputs:
Garbage is the number of outputs added to make an n-input k-output function reversible. We use the words constant inputs to denote the present value inputs that were added to an (n:k) function to make it reversible. The following simple formula shows the relation between the number of garbage outputs and constant inputs . Input + constant input = output + garbage. [6]

Quantum cost:
Quantum cost refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit. The quantum cost of a circuit is the minimum number of 2*2 unitary gates to represent the circuit keeping the output unchanged. The quantum cost of a 1*1 gate is 1 and that of any 2*2 gate is the same, which is 1 [10].

Table I. List of Reversible Gates

Reversible Gates	Size	Quantum cost	Functionality
NOT	**1X1**	1	P=A’
CNOT(Feynman)	**2X2**	1	P=A Q=AxorB
Fredkin	**3X3**	5	P=A Q=A’B+AC R=AB+A’C

Toffoli	**3X3**	5	P=A Q=B R=ABxorC
Pears	**3X3**	4	P=A Q=AxorB R=AB xor C
Double Feynman	**3X3**	2	
NG	**3X3**	11	P=A Q=AB xor C R=A'C' xor B'

2. IMPLIMENTATION DETAILS

In order to design reversible combinational circuits, the conventional logic gates are appropriately designed from the reversible gates to reduce quantum cost, garbage outputs and constant inputs. Table I gives the list of reversible gates available and their functionality as well as quantum cost. Report also discusses possible alternative solution to realize the same function. Figures 1 & 2 shows the NAND realization using either fredkin gate or peres respectively. Figures 3 & 4 shows the AND function using Fredkin gate and peres gate respectively. Figures 5 & 6 shows OR and NOR function using fredkin gate. Figures 7,8 and 15 shows how single reversible gate is used to realize multiple conventional gates. Feynman Gates [8] are also used for copying the outputs and to avoid the fan out problem in reversible logic. In the Feynman gate, there are exactly two outputs corresponding to the inputs and a 0 in the second input will copy the first input to both the outputs of that gate. Hence, it can be concluded that Feynman gate is the most suitable gate for single copy of bit, as it does not produces any garbage output as shown in figures 13 and 14. Using these basic gates reversible cost effective combinational circuits are built and discussed in next section.

2.1 Proposed Basic And Universal Gates Using Reversible Gates

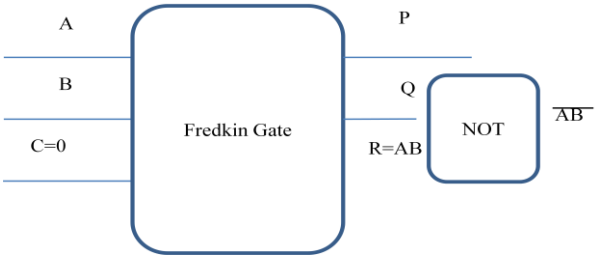

Fig. 1. NAND using Fredkin gate

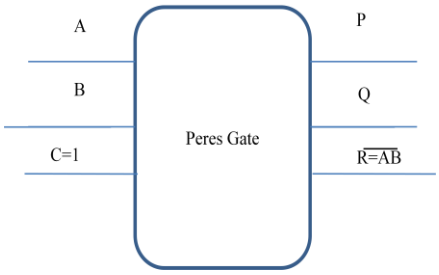

Fig. 2. NAND using Peres gate

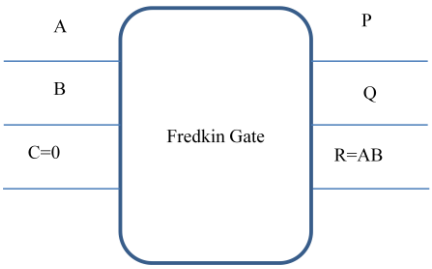

Fig. 3. AND using Fredkin gate

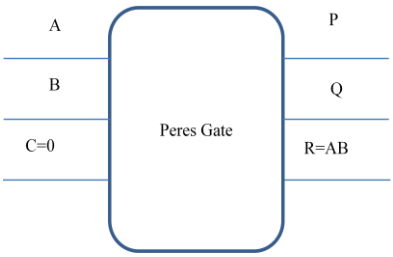

Fig.4. AND using Peres gate

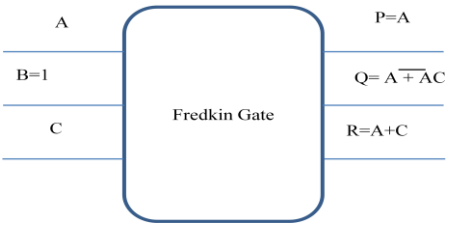

Fig.5. OR using Fredkin gate

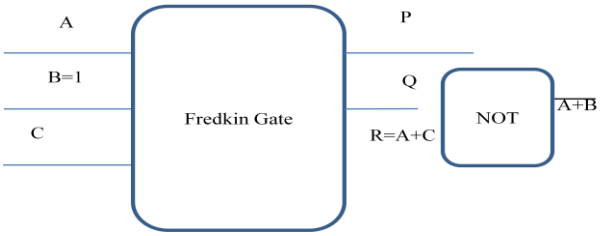

Fig.6. NOR using Fredkin gate

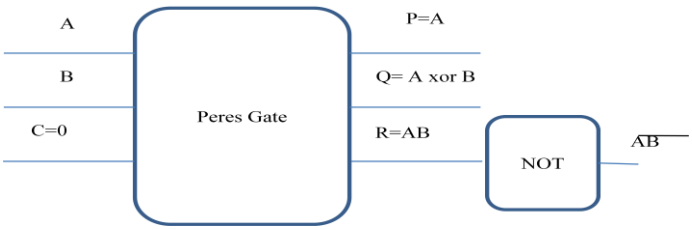

Fig.7. XOR, NAND and AND using Peres gate

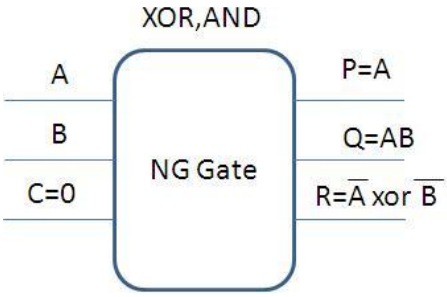

Fig.8. XOR and AND using NG gate

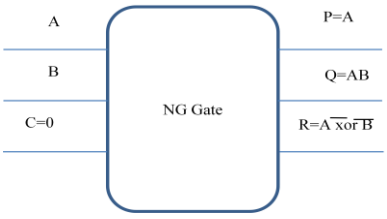

Fig.9. XOR and OR using NG gate

Fig.10. NAND and complement using NG gate

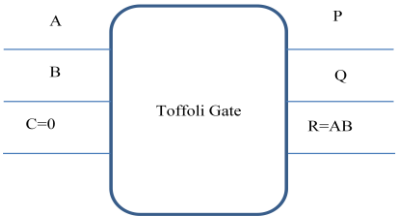

Fig.11. AND using Toffoli gate

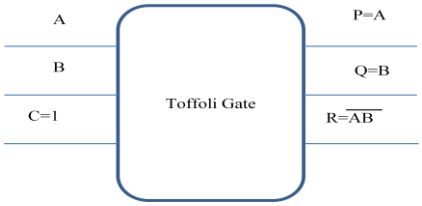

Fig.12. NAND using Toffoli gate

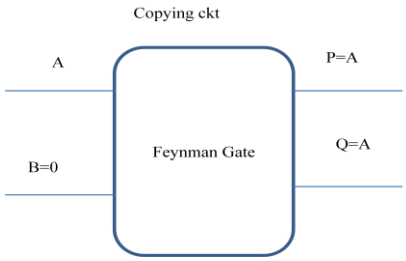

Fig.13. Feynman as a copying gate

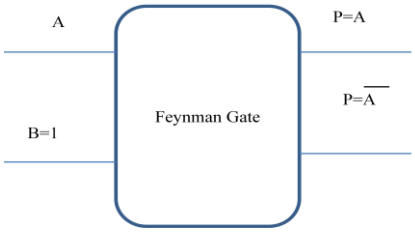

Fig.14. Feynman for complement gate

Fig.15. NG for NAND and complement gate

2.2 Proposed Combinational Circuits Using Reversible Gates

Adder and subtractor circuits are basic building blocks of any computing machine. Attempt is made here to realize cost effective reversible half, full adder and subtractors as shown in figures 16,17,18 and 19 respectively. Furher 2:1, 4:1 multiplexers and 1:4 Demux circuits also realized using reversible gates as shown in figures 20,21,22 and 23. Design of 4:2 encoder and 2 bit comparator is shown in figure 24 and 25.

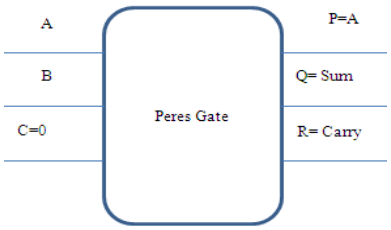

Fig.16. Half adder

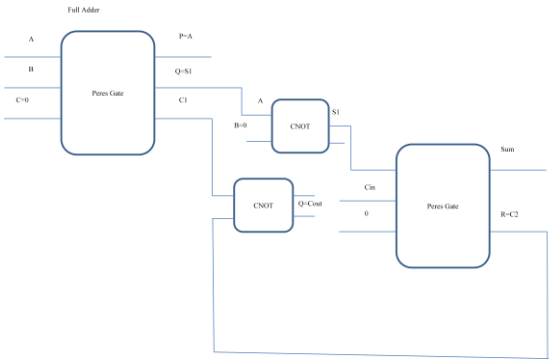

Fig.17. Full adder

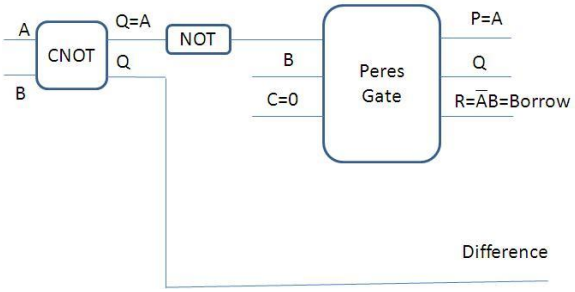

Fig.18. Half subtractor

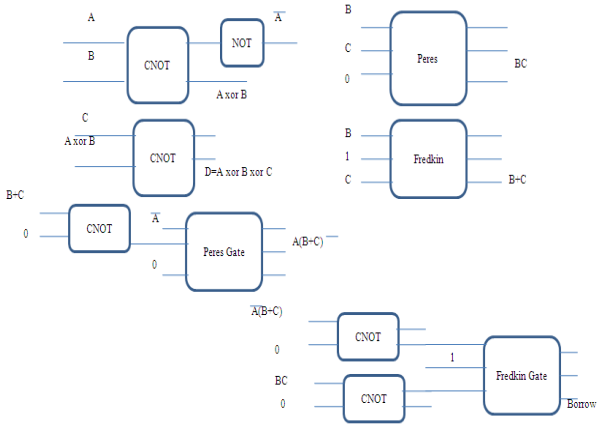

Fig.19. Full Subtractor

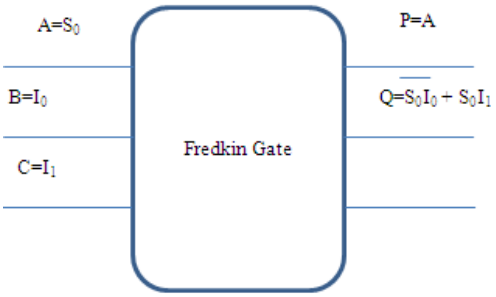

Fig.20. 2:1 mux

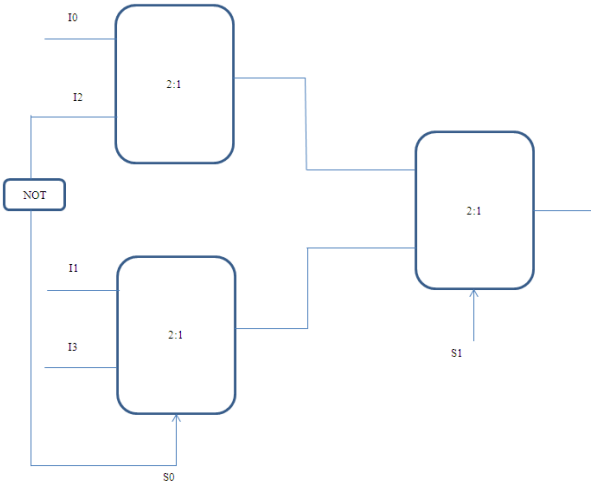

Fig.21. Conventional 4:1 mux

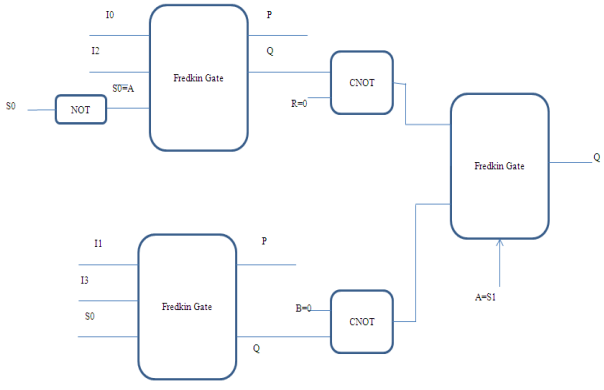

Fig.22. 4:1 Mux using reversible logic

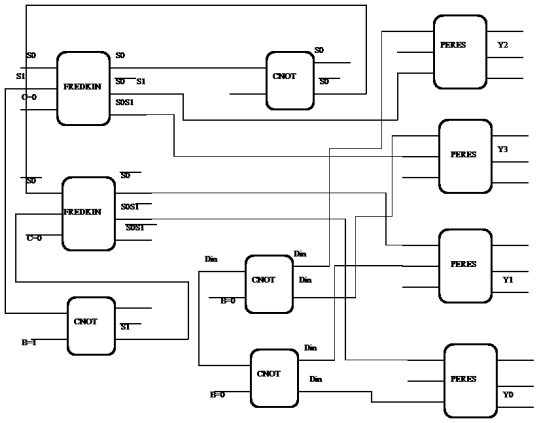

Fig.23. 1:4 Demux using reversible logic

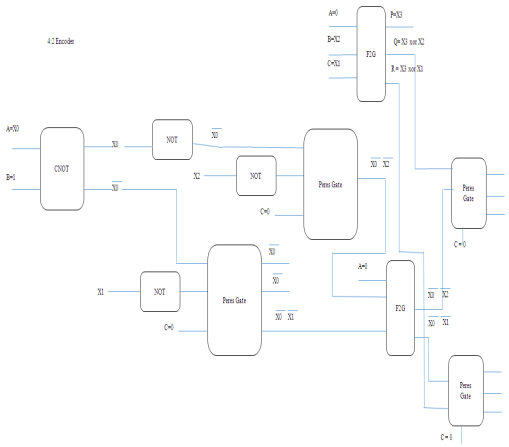

Fig.24. 4:2 Encoder

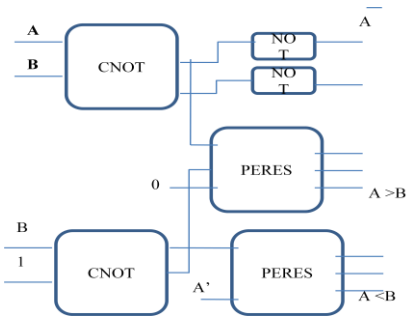

Fig.25. 2bit Comparator

3. RESULTS AND DISCUSSIONS

Proposed circuits using reversible gates are verified using Xilinx14.2 tool by developing verilog code and implemented on Spartan3 FPGA kit. Figures from 26 to 29 shows simulated results of half adder, full adder, half subtractor and full subtractor respectively. Simulated results of 2:1 and 4:1 mux is shown in figures 30 and 31. Figures 32 , 33 and 34 shows the results of 1:4 demux, 4:2 encoder and 2 bit comparator. TableII shows the summery all proposed circuits in this paper and respective performance parameters like quantum cost, garbage output and constant inputs. Attempt is made here to build combinational circuits using reversible gates which has minimum quantum cost.

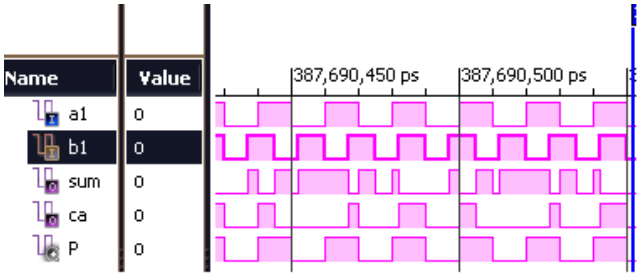

Fig. 26. Half Adder.

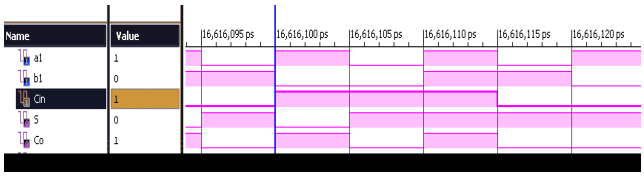

Fig. 27. Full Adder.

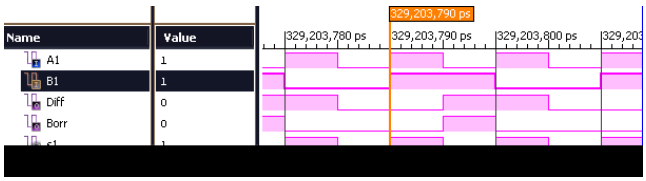

Fig. 28. Half Subtractor.

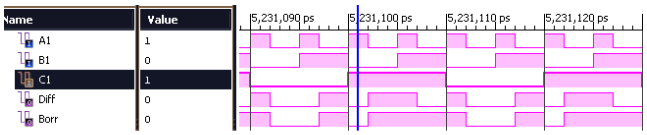

Fig. 29. Full Subtractor.

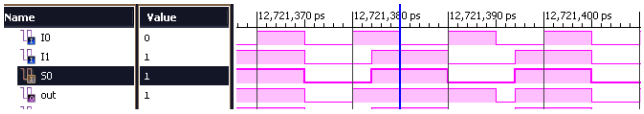

Fig. 30. 2:1 mux

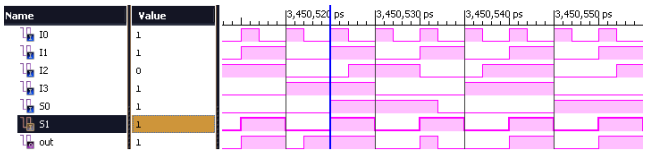

Fig. 31. 4:1 mux

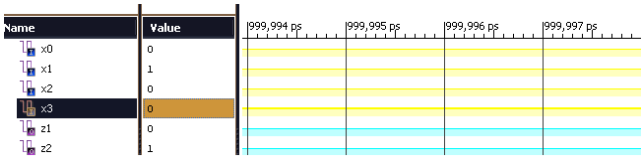

Fig. 32. 4:2 Encoder

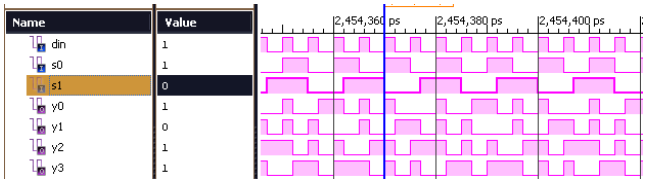

Fig. 33. 1:4 Demux

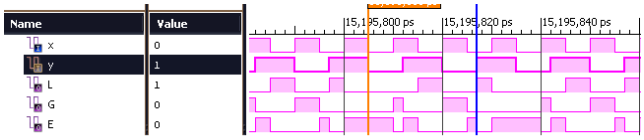

Fig. 34. 2 bit comparator

Table II. Summary of proposed circuits

Logic circuits proposed	Reversible gates used	Quantum Cost	Garbage outputs	Input(ancilla) constants
NAND	Peres	4	2	1
	Fredkin	6	2	1
AND	Peres	4	2	1
	Fredkin	6	2	1
OR	Fredkin	5	2	1
NOR	Fredkin	6	2	1
XOR,AND,NAND	Peres,NOT	5	1	1
XOR,AND	NG	11	1	1
NAND,Complement	NG	11	1	1
XOR,NOR	NG	11	1	1
AND	Toffoli	5	2	1
NAND	Toffoli	5	2	1
Copying circuit	Feynman or CNOT	1	0	1
Half adder	Peres	4	1	1
Full adder	Peres,Cnot	10	4	3
Half Subtractor	Peres,Cnot	6	2	1
Full Subtractor	Cnot,not,Peres, Fredkin	23	8	7
2:1 Mux	Fredkin	5	2	0
4:1 Mux	Fredkin, Cnot	17	7	2
4:2 Encoder	Cnot,double Feynman,Peres, Not	24	9	6
1:4 Demux	Peres,Fredkin, Cnot	30	11	10
2 bit comparator	Cnot,Peres,Not	12	4	3

4. CONCLUSION

This paper proposes design of conventional basic, universal gates and few combinational circuits like adders, subtractors, mux/demux, encoder and comparators using reversible logic. Attempt is made to realize these with minimum quantum cost, garbage outputs and delay so that any complex digital applications can be made more optimized. All circuits are simulated using xilinx 14.2 and implemented on Spartan3 FPGA development kit. Paper also discusses how Feynman gate is used for generating complement output and as a copying circuit.

5. REFERENCES

[1] R. Landauer, "Irreversibility and Heat Generation in the Computational Process," IBM Journal of Research and Development, 5, pp. 183-191, 1961.

[2] C.H. Bennett, "Logical Reversibility of Computation,IBM J.Research and Development," pp. 525-532, November 1973.

[3] Vlatko Vedral, Adriano Bareno and Artur Ekert, "QUANTUM Networks for Elementary Arithmetic Operations," arXiv:quantph/ 9511018 v1, Nov 1995.

[4] A. Mishchenko, M. Azad Khan, A. Coppola, S.Yanushkevich, "A general decomposition for

reversible logic," IEEE transactions Proc. RM2001, Starkville, pp: 119-138, 2001.

[5] Haz Md. Hasan and A.R. Chowdhury, "Design of Reversible Binary Coded decimal Adder by using Reversible 4 bit Parallel Adder," IEEE Trans. Very Large Scale Integr. (VLSI) Jan. 2005. B.Raghu kanth, B.Murali Krishna, M. Sridhar, "A DISTINGUISH BETWEEN REVERSIBLE AND CONVENTIONAL LOGIC GATES," International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com Vol. 2, Issue 2,Mar-Apr 2012, pp.148-151

[6] Abu Sadat Md. Sayem, Masashi Ueda, "Optimization of reversible sequential circuits Journal of Computing," Volume 2, Issue 6, June 2010, ISSN 2151-9617.

[7] H.Thapliyal and N. Ranganathan, "Design of reversible sequentialcir-cuits optimizing quantum cost, delay and garbage outputs," ACM Journal of Emerging Technologies in Computing Systems, vol. 6, no.4, Article 14, pp. 14:114:35, Dec. 2010.

[8] J.Smoline and David P.DiVincenzo, "Five two-qubit gates are su cient to implement the quantum fredkin gate Physics Review A," vol. 53, no.4, pp. 2855-2856,1996.

[9] Yang G., Song X, Hung WNN, and Marek Perkowski, "Bi-direction Synthesis for Reversible circuits," IEEE Computer Society Annual Symposium on VLSI New Frontiers in VLSI Design, 2007.

[10] D. Maslov and G.W. Dueck, "Reversible cascades with Minimal Garbage," IEEE Transactions on CAD, vol. 23(11), pp. 1497-1509, November 2004.

[11] Richard P.Feynman, "Quantum mechanical computers Foundations of Physics," vol.16, no. 6, pp.507-531,1986.

[12] H. Thapliyal and M. B. Srinivas, "A Beginning in the Reversible Logic Synthesis of Sequential Circuits," Proceedings of Military and Aerospace Programmable Logic Devices International Conference, 2005.

[13] S.K.Sastry, H.S.Shroff, S. N. Mahammad, and V. Kamakoti, "Efficient building Blocks for Reversible Sequential Circuit Design," *In Proc. the 49th IEEE Intl. l Midwest Symp.on Cir.and Sys*., pages 437–441, Puerto Rico, Aug. 2006.

[14] J.E. Rice , "A New Look at Reversible Memory Elements," Proceedings of IEEE International Symposium on Circuits and Systems, 2006.

[15] V. Rajmohan , "Design of Counters Using Reversible Logic," Member IACSIT978-1-4244-8679 2011 IEEE

[16] H. Thapliyal and A. P. Vinod , "Design of reversible sequential elements with feasibility of transistor implementation," In Proc. the 2007 IEEE Intl. Symp. On Cir.and Sys., pages 625628, New Orleans, USA, May 2007.

[17] Ashis Kumer Biswas, La fa Jamal, M. A. Mottalib1, Ha z Md. Hasan Babu , "Design of a Reversible Parallel Loading Shift Register," Dhaka Univ. J.Eng and Tech. vol 1(2) 1-5,2011.

[18] D. Krishnaveni, M. Geetha Priya , "A Novel Design of Reversible Uni-versal Shift Register with Reduced Delay and Quantum CostJournal of Computing," Volume 4, Issue 2, February 2012, Issn 2151-9617.l

[19] Md. Selim A Mamun, Indrani Mandal, Md. Hasanuzzaman , "Design of Universal Shift Register Using Reversible Logic," IJET Publications UK. All rights reserved September, 2012.