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Simplification of Ternary Function using Variable Entered Mapping Technique

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ABSTRACT
This paper describes the steps for minimization of ternary function i.e. three level logic using variable entered mapping technique. Here we applied VEM technique successfully to the ternary function and result is verified using truth table of given ternary equations. We also implemented simplified expression using decoder and ternary gates as well as using ternary multiplexer.

It will be more difficult as radix of the number system increases to get more difficult in minimization and to design circuit.

In this paper we successfully applied VEM technique to ternary system, the proposed technique is developed for the ternary logic function simplification. It incorporates all designed rules for ternary logic system design and gives the output in the form of Sum-of-Product (SOP) terms.

Generally VEM technique is used for the minimization of binary function so the rule used here are different than binary logic. Output equation of ternary digital system is in the form of F = F2 + 1. (F1) Where, F2 = 2's minterms and F1 = 1's minterms.

Keywords
Multivalued logic,(MVL) Radix; Sum-of-Product (SOP); Ternary;,T-gate MEV, Unary function.

1. INTRODUCTION
Today's digital technology based on binary system. Shannon expressed the behavior of electrical switches in Boolean algebra he overlay the ramp to an industrial development which is recognized as beginning of one of the most revolutionary economic changes ever.

Due to recent development in binary logic technology has come across the dramatic changes and advances. Electronic tubes like Triode are used instead of electromechanical switches in (1919) then from tubes to transistors (1948) and from transistors to LSI (1958) and VLSI (1970) circuits. Binary logic is not most efficient and powerful switching logic. Multiple value logic (radix>2) has introduced. In case of 3- valued logic (radix=3) term ternary logic is used and for radix=4 term quaternary is used. Ternary logic represented three levels and it switches between three states.

For ternary logic system there are three states '0','1','2',and 4-value switch with logic states '0', '1', '2' and '3' and so on up to 'n' values. In MVL there are three directions for the work. First is to reduce chip area in VLSI and reduce interconnection complexity. It gives motivation for the investigation of many hardware implementations of MVL system.

Most important commercial application of MVL is area of MVL memories. The MVL can be used to overcome existing difficulties in the analysis of problems in binary digital systems, such as the design of fault simulators. Finally there is still ongoing work in the general area of switching theory to yield the best methodologies for the implementation of multi-valued systems.

There are three directions for the work in MVL. Due to pressure to reduce interconnection complexity and reduce chip area on VLSI, it is giving motivation for the investigation of many different hardware implementations of MVL systems. The largest commercial use of Multiple-Valued logic is in the area of MVL memories. The MVL can be used to overcome existing difficulties in the analysis of problems in binary digital systems, such as the design of fault simulators. Finally there is still ongoing work in the general area of switching theory to yield the best methodologies for the implementation of multi-valued systems.

1.1 History Of Ternary Logic
In existing binary digital system, the output of the system is decided by considering two input conditions i.e. either ON (Favorable or true logical level 1) or OFF (unfavorable or false logic at logic level 0) leaving behind the third conditions i.e. when both the input conditions are same, here decision is consider as don't care or it is discarded by the system. Such situation generally occurs in sequential circuit design. Consider a digital system where both the inputs are same i.e. either 00 or 11.

In binary system output will be uncertain or will be same as that of previous state of the system but in practice, system must give the output that will satisfy both the input conditions mentioned above. The system gives the output which is balanced and this state is regarded as third state i.e. can't say or can't make any decision. So to make third decision the radix of the system must be greater than 2. Here the third logic level is introduced whose system radix is greater than 2. Alexander [1964] showed that natural base (e= 2.71828) [1] is the most efficient radix. for implementation of switching circuits. It seems that most efficient radix for the implementation of digital system is 3 than 2. Ternary logic system, meaning that it has 3 valued switching. Ternary system has several important merits over binary. It can be

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listed as reductions in the interconnections require to implement logic functions, thereby reducing chip area, more information can be transmitted over a given set of lines, lesser memory requirement for a given data length. Besides this serial & some serial-parallel operations can be carried out at higher speed [1-3]. Its advantages have been confirmed in the application like memories, communications and digital signal processing etc [12].

2. TERNARY BOOLEAN ALGEBRA

Let a system be L whose elements called propositions or statements are valued in the set {0, 1, and 2} which is denoted by Z3. If X is a proposition, the value of X can be seen as a mapping $V: L \rightarrow \{0, 1, 2\}$ such that

$$V(x) = \begin{cases} 0 & \text{if X is false} \\ 1 & \text{if X is intermediate} \\ 2 & \text{if X is true} \end{cases}$$

Ternary has the logic levels '0' corresponding to logic-0 in binary (also called zero element or low voltage), '1' corresponding to an intermediate stage (also called Meta stable state) and '2' corresponds to logic-1 in binary (Also called universal element or high voltage). The intermediate state can be metaphorically thought of as either true or false. The binary logic is limited to only two states '1' and '0', where as MVL is a set of finite or infinite number of values. In a standard CMOS process, the three supply voltages are vdd, vdd/2 and ground.

Ternary logic gates are the basic building blocks in realizing combinational and sequential logic functions. The implementation is based around (bipolar transistors, MOSFETs etc.) a basic switching elements, which is Referred to as T-Gates [8] the Ternary gate called T-gate qualifies as a universal element in several different senses. Firstly, it should be logically complete with simple operation. Secondly, it should be easily implemented with its straightforward construction. Thirdly, it should possess two essential elements that must be embodied in any logic gate, namely, logic-value thresholding and logic-signal connection of switching [15]. This functional completeness of T-gate is the property of a set of compositions which enables one to synthesize any arbitrary switching function within a particular class. There are several algebras available for the design of ternary switching functions among which, the Post and the Modular algebra have the advantages of similarity with ordinary algebra. In system L, a set of operators namely unary and binary are defined.

For x, y, z € L, there exists an equivalence (=) operation, such that

x = x

If x = y, then y = x

If x = y and y = z, then x = z

When n = 1, one-variable functions f(x) exist with $3^{3^1} = 27$ modal functions called Literals as shown in Table I. Similarly, there are $3^{3^2} = 19683$ two-variable functions and $3^{3^3} = 76255974849$ three-valued functions Literal is denoted by a $X_{i,}^{a}$ where $a_I = 0,1,2,01,02$ and 12 and is defined as given below

$$X^I = \begin{cases} 0 & \text{if } X \neq I \\ 2 & \text{if } X = I \end{cases}$$

Where I = 0, 1&2

$$A^{01} = A^0 + A^1 \quad (1)$$

$$A^{12} = A^1 + A^2 \quad (2)$$

$$A^{02} = A^0 + A^2 \quad (3)$$

$$A^{01} \bullet A^{12} = A^1 \quad (4)$$

$$A^{01} \bullet A^{02} = A^0 \quad (5)$$

$$A^{02} \bullet A^{12} = A^2 \quad (6)$$

$$A^0 + A^1 + A^2 = 2 \quad (7)$$

Table 1. Function Table of Unary Functions

A	A^o	A^1	A^2	A^{o1}	A^{12}	A^{o2}
0	2	0	0	2	0	2
1	0	2	0	2	2	0
2	0	0	2	0	2	2

It can be proved that the complement or negation of literals (X^1) give the following observed in Equations which are helpful in reduction of ternary gates during implementation

$$COM(X^i) \text{ or } NEG(X^i) = x^I = 0 \text{ if } X=I \quad (8)$$

$$A^2 = A^{01} \& A^{01} = A^2 \quad (9)$$

$$A^1 = \overline{A^{02}} \& \overline{A^{02}} = A^1 \quad (10)$$

$$A^0 = \overline{A^{12}} \& \overline{A^{12}} = A^0 \quad (12)$$

$$\bar{0} = 2 \& \bar{2} = 0 \quad (13)$$

This observed result is used to show the reduction in gate count and also in simplification of ternary function.

The operation of addition (+) and multiplication (.) on L, which can be called Ternary OR (TOR) and Ternary AND (TAND) respectively, represent two multiple input operators. It is represented by following equations

Logic Sum or TOR:

$$A1A2\ldots An = MAX(A1, A2, An) \quad (14)$$

Logic Product or TAND:

$$A1 + A2 + \ldots + An = MIN(A1, A2, \ldots An)$$

Similarly, TNAND is

$$\overline{A1 \bullet A2 \bullet \ldots \bullet An} = MIN(\overline{A1 \bullet}, \overline{A2 \bullet} \ldots \bullet An) \quad (15)$$

$$\overline{A1 + A2 + \ldots + An} = MAX(\overline{A1} + \overline{A2} + \ldots + \overline{An}) \quad (16)$$

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Clearly (L, +,) is a distributive lattice with zero element (0) and universal element (2) Thus the following laws hold for any x, y, z ∈ L:

Idempotent: A+A=A

A ● A=A

Commutative: A+B=B+A

A ●B=B● A

Associative: (A+B) +C=A+ (B+C)

A● (B ● C) = (A ●B) ●C

Absorption: A+ A●B =A

A● (A+B) = A

Distributive: A+B●C= (A+B) ● (A+C)

A● (B+C) =A●B+A● C

It is evident that laws of identity elements, holds here.

$A + 0 = A$ (17)

$A \bullet 0 = 0$ (18)

$A + 2 = 2$ (19)

$A \bullet 2 = A$ (20)

$A \bullet 1 = 1$(for cases $A \neq 0$) (21)

$A+1 = 1$(for cases $A \neq 2$) & 2(for A=2) (22)

DeMorgan's Theorem holds for ternary logic when the three types of inverters are used

$\overline{(A+B)}^{o} = \overline{A}^{o} \bullet \overline{B}^{o}$ (23)

$\overline{(A \bullet B)}^{o} = \overline{A}^{o} + \overline{B}^{o}$ (24)

$\overline{(A \bullet B)}^{1} = \overline{A}^{1} + \overline{B}^{1}$ (25)

$\overline{(A+B)}^{1} = \overline{A}^{1} \bullet \overline{B}^{1}$ (26)

$\overline{(A \bullet B)}^{1} = \overline{A}^{1} + \overline{B}^{1}$ (27)

$\overline{(A+B)}^{2} = \overline{A}^{2} \bullet \overline{B}^{2}$ (28)

$\overline{(A \bullet B)}^{2} = \overline{A}^{2} + \overline{B}^{2}$ (29)

$\overline{\overline{A}^{1}}^{1} == A$ (30)

Ternary functions of one or more variables may be represented in truth table or K-map form or algebraically in canonical form as a product of sum or sum of product. According to Expansion theorem [14] any ternary function f(Xl,X2,...,Xn) may be generated from (Xl, X2,...,Xn) by means of (+), (.) and the unary functions X 0 , X 1 , X 2 as given below

f(Xl,X2, , Xn) = 2 • F2(Xl,X2 ..... Xn)+1 •F1(Xi, X2, ...,x n)+0•F0(Xl,X 2... Xn)

i.e, f = 2 • F2 + 1 • F1 + 0 • F0 (31)

Where Fk equals 2, when value of the function f equals k, otherwise, it is 0. Applying equations (21) and (23)

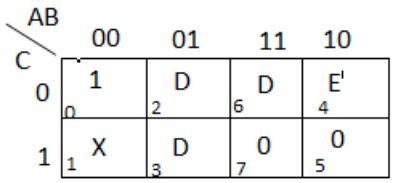
To the above equation, the function may be represented by f = F2+1 • F1 for canonical Sum of Product form and f= F2 • (1+ F1) for canonical Product of Sum form

3. VARIABLE MAPPING TECHNIQUE

A VEM is a k-map method that has some variable from function appearing in the cell of map consider following function

F=A`B`C`+BC`D+A`BCD+AB`C`E`+d (A`B`C)

Above function plotted on three variable k-map that has A,B,C are the inputs and D and E uses map entered variable(MEVs) To enter product term for the above function proceeds as follows. The term A`B`C` does not depend upon D or E so place 1 in cell 0. The term BC`D depend upon D so place D in cell 2 and 6. The term A`BCD again depends on D so place D in cell 3.Similarly place E` in cell 4 and don`t care in cell 1



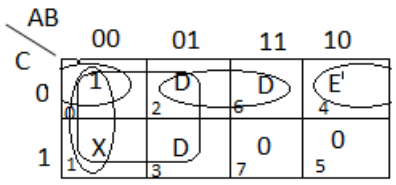
STEPS FOR VEM

1) Consider all MEVs are o and loop 1 then identifies essential group and read map as usual.

2) For each MPV form loops containing only the MPV 1's and don't care. Treat 1s as a don't care when looping MEVs.Also treat MEV and complement of that MEV as they were independent variables.

3) Finally find essential prime implicant for MEVs and read minimum expression from k-map as usual. All MEVs covered by some loop. A loop containing an MEV is read as usual and then the MEV ANDed to the minterm.

Map for above example is



F=A`B`+A`D+BC`D+B`C`E`

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4. MINIMISATION OF TERNARY FUNCTION USING VEM METHOD

Many researcher developed method for minimization using Boolean algebra for ternary logic. As well as k-map technique for ternary logic. We proposed variable entered mapping technique for ternary function.

There are some rules or protocol for joining adjacent cell for minimization of ternary function.

1) The group of 3×1, 3×2, 3×3 cells can be formed to provide simplified term.

2) It is allowed to join adjacent cell with equal values.

3) Multiple uses of cell for different purpose is allowed.

4) Here 2 can be considered as a don't care for grouping of 1.

5)For variable entered mapping enter last variable of each term in to map

Output equations of ternary digital system is in the form of F1 and F2 terms i.e.

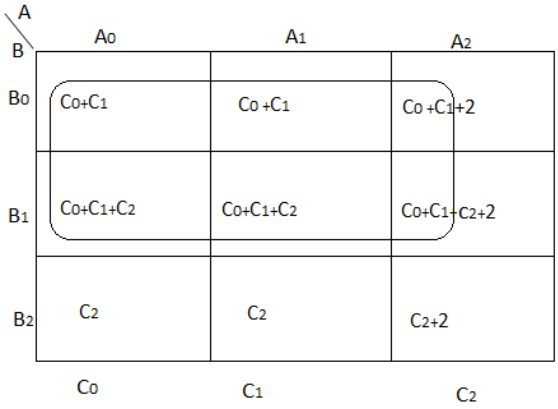
F=f2+1.f1 where

F2= 2's minterm

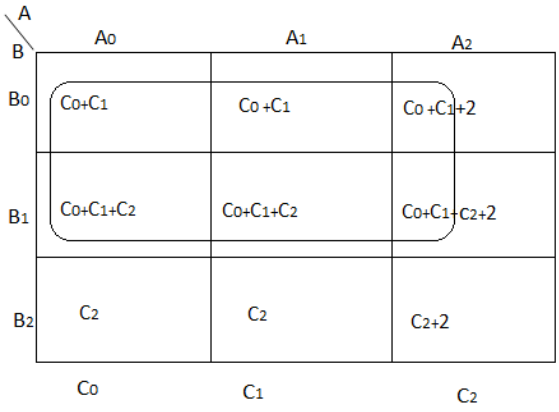
F1= 1's minterm

$F=A_0B_0C_{0+}\ A_0B_0C_{1+}\ A_1B_0C_{1+}\ A_1B_0C_{0+}\ A_2B_0C_{1+}\ A_2B_0C_{0+}\ A_0B_1C_{1+}\ A_0B_1C_{0+}\ A_0B_1C_{2+}\ A_2B_{0+}\ A_1B_1C_{0+}\ A_1B_1C_{1+}\ A_1B_1C_{2+}\ A_2B_1C_{0+}\ A_2B_1C_{1+}\ A_2B_1C_{2+}\ A_0B_2C_{0+}\ A_1B_2C_{2+}\ A_2B_2C_2+A_2B_{1+}A_2B_{2+}1(A_0B_0C_{0+}\ A_0B_0C_{1+}\ A_2B_0C_{1+}A_0B_2C_{2+}\ A_1B_2C_{2+}\ A_2B_2C_2)$

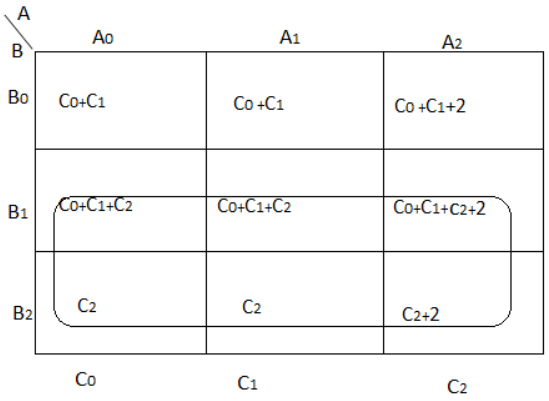
In this case enter C_0, C_1, C_2 in to map, First group is taken for variable C_0



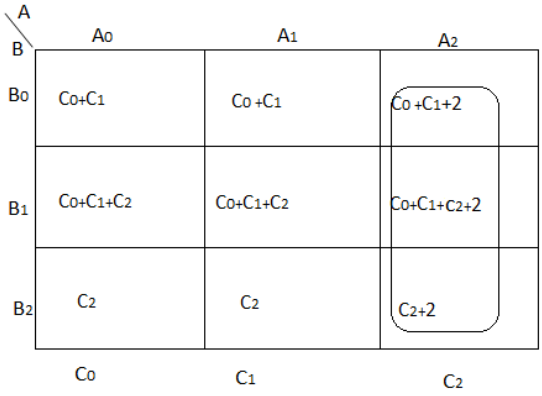
, And same is the group for variable C_1 i.e. 6×1



Group of variable C_2 is 6×1



Similarly group of 2 i.e. 3×1



Simplified term for group 1 2 and 3 is

$F_2 = C_0+C_1+C_2+A_2$

And map for 1s minterm is

Here two group of 3×1

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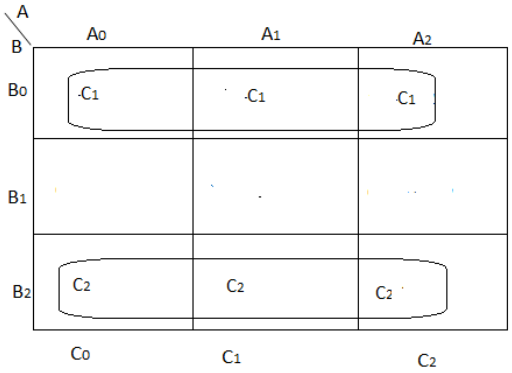


Term is $F_1 = C_1+C_2$

Complete simplified expression is

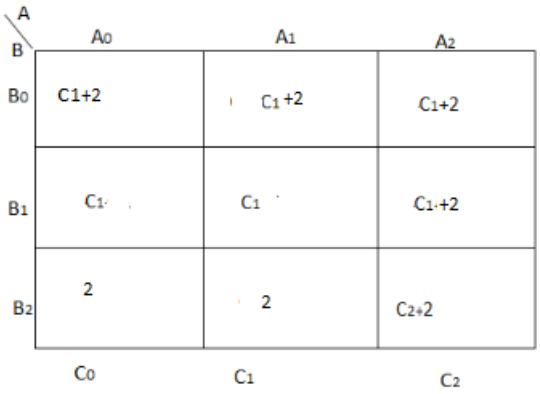
$$F = F_{2+}1F_1$$

$$F = C_0+C_1+C_2+A_2+1(C_1+C_2)$$

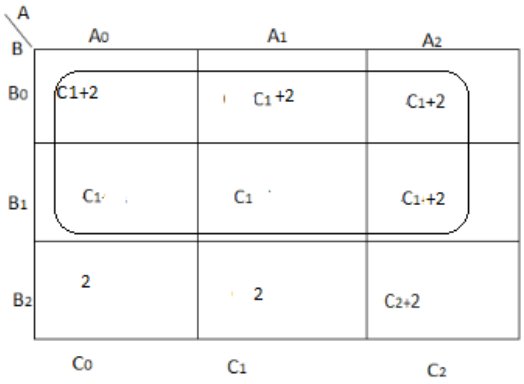
Example 2: Given ternary expression is

$F=A_0B_0C_{1+}\ A_1B_0C_{1+}\ A_2B_0C_{1+}\ A_0B_1C_{1+}\ A_1B_1C_{1+}\ A_2B_1C_{1+}\ A_0B_{0+}\ A_1B_{0+}\ A_2B_{0+}\ A_0B_{2+}\ A_1B_{2+}\ A_2B_2\ {}_+1(A_0B_{0+}\ A_1B_{0+}\ A_2B_{0+}A_0B_{2+}\ A_1B_{2+}\ A_2B_2)$

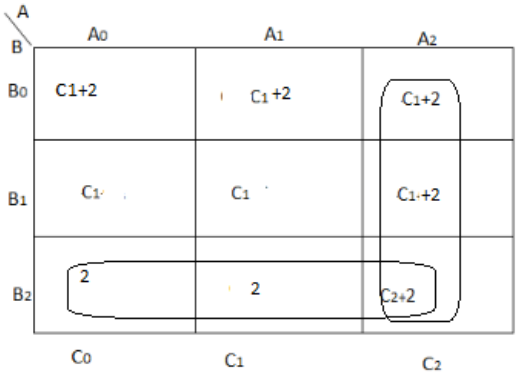
Map for equation is



Case 1:Map for 2,s minterm, and Grouping of variable C_1



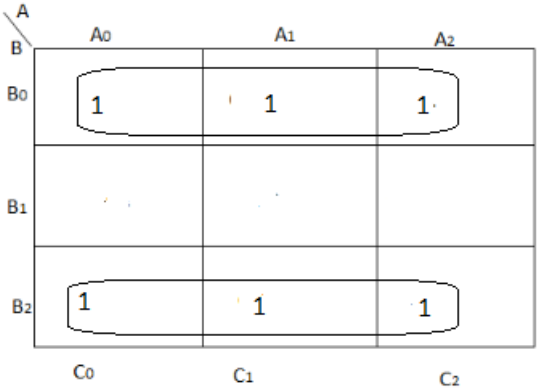
Grouping of 2's 3×1



Simplified terms are

$$F_{2=}\ C_1+B_0+B_2+A_2$$

Case2: grouping of 1's minterm



Terms for above group is

$$F_{1=}B_0+B_2$$

Total simplified expression is

$$F = F_2+1F_1$$

$$F = C_1+B_0+B_2+A_{2+}1(B_0+B_{2)}$$

Implementation of above simplified function using decoder and ternary gate is [21]

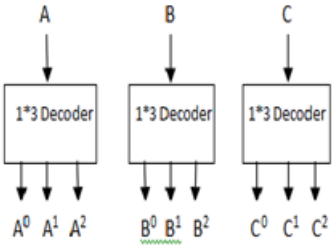


Figure1: **ternary 1*3 decoder**

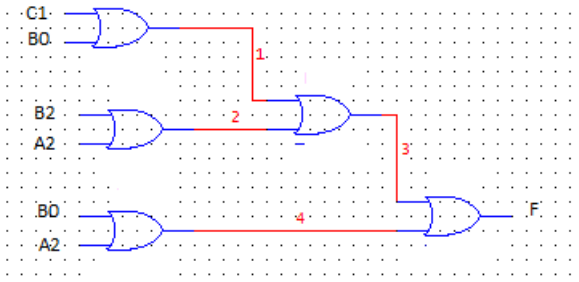


Figure 2: **implementation of simplified equation using tor gates**

5. RESULT AND DISCUSSION

A ternary function simplified by variable entered mapping technique gives simplified solution. This paper describe minimization of two ternary function using variable mapping technique successfully We can verified result by using k-map technique which is found to be correct .This technique is useful when number of variable in ternary expression increases. We implemented given expression and simplified expression using ternary gate and found that very less number of gates required for simplified equation

	Number of ternary decoder	Number of Tand gate	Number of Tor gate	Total gate required
Example 1	3	27	13	40
Simplified expression1	3	----	4	4
Example 2	3	18	9	27
Simplified expression2	3	---	4	4

6. APPLICATION

Plenty of applications over MVL system have been developed earlier [9]. A set of simultaneous equations in Boolean algebra are required for obtaining the minimization technique. Variety of applications can be developed easily using these minimization techniques to reduce the solution. Boolean equations used in this operations research are referred to in [8]. Reducing the complexity of the circuit is the major objective behind this research. Development of calculus for the multivalued logic algebra system is one such example

7. CONCLUSION

A ternary function simplification by a variable entered mapping method is gives simplified solution. This paper describes how to get minimized solution if more number of variable given in multiple value expression.

Here same result is verified using k-map technique and found to be correct. It is suggested that by using same rule and algorithm this method is applicable to higher radix for future scope.

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