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A 953nw, 0.8V, 27ppm/ºC, Nano Power CMOS Voltage Reference Circuit

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ABSTRACT
In the field of power-aware applications, like smart sensors, wearable medical devices, required low supply voltage for operation. The supply voltage should be insensitive to temperature variation and line variation and power consumption in order of few micro watts. To achieve this requirements a Nano-power CMOS circuit is designed. It generates a constant reference output voltage working with a supply voltage ranging from 0.8V to 1.8V. Circuit was simulated in $0.18\mu m$ UMC CMOS process. It generate a reference voltage of 400mV at 0.8 V supply at room temperature. A proper sub-threshold design operation of the circuit allow us to work at absolute temperature with operating voltage 0.8V and current drawn from the supply was 1.2 µA. The temperature coefficient calculated in temperature from $-30℃$ to 80℃ is $27ppm/℃$ and the measured line sensitivity was$0.132\%/V$.The measured (PSRR) was -39 dB at 100Hz and -40 dB at 10MHz respectively.

Keywords
Sub threshold, Low power, Low voltage, Power supply rejection ratio, Temperature coefficient,

1. INTRODUCTION
Voltage reference circuit is the basic building block of analog circuits. It provides reference output voltage for circuits. In the literature different type of reference circuits were reported. The first reference circuit was designed in 1971 by the WIDLAR on the principle of band gap reference. This circuit consists of vertical bipolar transistor and large value of resistor for Low voltage application .So there is problem of area and power consumption in designing of LSIs in VLSI field. To resolve these problems many solution were reported in previous work. Most of the solution based on the principle of sub-threshold operation of MOSFETs and temperature compensation against the variation of mobility with temperature. In sub threshold region of operation the circuit works with low supply voltage. It may be less than 1 V. The power consumption was in order of few micro watts. There is a problem with sub threshold operation because in this region the circuit more sensitive to temperature variation and process variation. The circuit mostly affected by variation of threshold voltage with temperature and mobility variation with temperature. That means the circuits which worked on the principle of sub-threshold operation have less temperature compensation against the mobility. They have poor line sensitivity that means output reference voltage change with change in supply voltage due to unwanted noise voltage. I concentrate to improve the line sensitivity and temperature compensation on mobility and threshold voltage. I take as a reference paper of Ref. [6]. in this paper they use the concept of sub-threshold operation so the circuit work with supply voltage less than 1 V and power consumption was very less. The circuit designed in this paper good for low voltage and low power application but more sensitive to temperature variation and line variation. For this problem, we designed a new voltage reference circuit that operate in the both region of operation saturation and sub-threshold at same time of operation by using different threshold voltage MOSFETs, high threshold MOSFETs and low threshold MOSFETs. The circuit will work well if we select the physical parameter of MOS properly. The circuit has good temperature compensation because most of the transistor operates in saturation region of operation and circuit will start to work above 0.8 V at room temperature. The circuit has less sensitivity against the temperature and line variation, the measured TC was 27ppm/ºC, line sensitivity was$0.132\%/V$. There is no problem of body effect and channel length modulation because all the MOSFETs bodies are grounded. It achieves better temperature compensation related to previous papers. This paper describes the operating principle in section 2, Circuit operation in Section 3, Results and discussion in Section 4, Conclusion in Section 5.

2. OPERATING PRINCIPAL OF PROPOSED CIRCUIT
The function of circuit based on three sub circuit's first start-up, second current generator, third active load. The function of start-up is provide proper operating condition for circuit and it avoid zero biasing condition, all the MOS transistor of start-up circuit will work in saturation region with supply voltage of 1.8 V. It has MOS transistors from $M_{1s} - M_{6s}$. The function of current generator is to generate the current. It consists of two current mirror circuits first $M_1 - M_2$ and second $M_3 - M_4$ and circuit from $M_1 - M_8$ work as a current generator. Third circuit is active load $M_9 - M_{10}$. It take the current from current generator circuit and generate reference output voltage across the transistorM_{10}. It works in the saturation region, the reference output voltage given by equation (1).

$$V_{REF} = V_{th10} + \sqrt{\frac{2I_0}{K_{10}}} \quad (1)$$

Where I_0 is the operating current of M_{10} .Equation (1), clear the temperature constant of the output reference voltage has two components first component due to the temperature sensitivity of the threshold voltage and a second component due to the temperature variation of mobility and of the bias current. Since K_{10} is linearly dependent to mobility, an

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operating current linearly dependent to mobility will help to completely vanish the effect of the temperature variation of mobility on the output reference voltage. As a linear approximation, we can think that the threshold voltage of an NMOS transistor proportionally decreases with temperature, as shown below:

$$V'_{TH}(T') = V'_{TH}(T_{01}) - K_{t1}(T' - T_{01}) \quad (2)$$

Where T' room temperature and T_{01} is the absolute temperature at which K_{t1} is calculated .To achieve the circuit will less sensitive to temperature variation with a complete cancellation of the temperature variation of mobility at any temperature, we required a operating current linearly dependent to $I_0 \propto \mu(T)T^2$ mobility and to squared of temperature that is, We achieve a solution to produce such a reference current with MOSFETs working in strong-inversion region and the weak- inversion region.

3. CIRCUIT DESCRIPTION

The designed voltage reference circuit is shown in figure 1. The core of the circuit made by transistor numbered from M_1 to M_9 produce a current I_0 as insensitive as possible of operating voltage V_{DD}. Such current is then enforced into the NMOS transistor M_{10}. Which is diode connected that means his gate terminal connected to his drain terminal so that it acts like a resistor in deep triode region and in saturation region it wok in saturation region in this circuit and generate reference output voltage. The temperature variation of I_0 is manipulated by the temperature variation of the gate-source-voltage, of transistor M10. It gives the temperature-compensated reference voltage V_{REF}.

3.1 Current generator Circuit

The function of current-sub circuit is to develop a temperature insensitive current. It consist the transistors numbered from $M_1$to M_4, they evaluate value of current (I_0) and MOS transistor M_6, M_5 inject same current (I_1) in M_3 and M_1 and transistor M_8, M_7 inject same current (I_0) in M_4 and M_2. Transistor M_1 and M_3 are high threshold MOSFETs and remaining MOSFETs are low threshold MOSFETs. The two different threshold MOSFETs will help us to operate M_3 and M_1 in sub threshold characteristics and, at the same time M_4 and M_2 work in saturation characteristics. Such behavior is accomplished by putting the source-gate voltages of M_2, M_1 and M_4, M_3 a value in between 0.5 V and 0.7 V. The (V-I) operating principle of an N MOS transistor that work in the Saturation characteristics and the sub-threshold characteristics can be given by (3) and (4), respectively.

$$I_D = \mu C_{ox} \; V_T^2 \frac{W}{L} e^{\frac{Vgs-Vth}{mVT}} \left[1 - e^{-\frac{Vds}{VT}}\right] \quad (3)$$

$$I_D = \frac{\mu C_{ox}}{2} \frac{W}{L} (Vgs-Vth)^2 (1+\lambda V_{DS}) \quad (4)$$

V_T - thermal voltage, m is the sub-threshold slope parameter. The source-gate voltages of M_2 and M_1 (M_4 and M_3) are equal and can be calculated from (2) and (1) by taking M_3 and M_1 in sub-threshold for drain current (I_1) and M_4 and M_2 in saturation for a drain current (I_0). By imposing $V_{gs3} = V_{gs4}$ and $V_{gs2} = V_{gs1}$, we have

$$I_0 = \frac{\mu C_{ox} \frac{W}{L}}{2(N-1)^2} \; m^2 \; V_T^2 \; ln^2\left(\frac{\frac{W_3}{L_3}}{\frac{W_1}{L_1}}\right) \quad (5)$$

Where we have defined $N = \sqrt{\frac{\frac{W_4}{L_4}}{\frac{W_2}{L_2}}}$

Here we have not consider channel-length modulation (λ=0), and have put the second term in equation (2) to unity. There is no problem of body effect because the source terminals of all NMOS transistor are connected to ground, and $V_{th4}=V_{th2}$ and $V_{th3}= V_{th1}$.

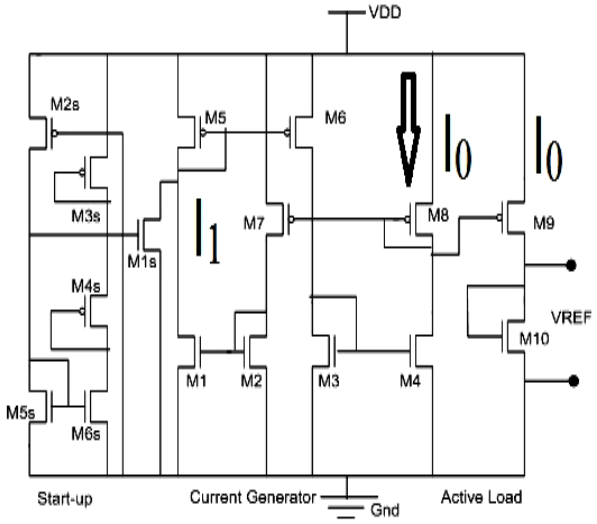

Fig.1. Voltage Reference Circuit

3.2 Active Load

It has a MOS transistor M_{10} , gate and drain terminal of this MOSFET connected together like a diode-connection. The current generated by equation (5) is enforced into diode – connected MOS transistor M_{10}, for achieving a temperature insensitive reference output voltage .M_{10} works in the saturation characteristics, by the application of (4) and (5), we can achieve the output voltage $V_{REF.}$

$$V_{REF} = V_{th10} + \frac{mV_T}{N-1} \sqrt{\frac{\frac{W_4}{l_4}}{\frac{W_{10}}{L_{10}}}} \ln\left(\frac{\frac{W_3}{L_3}}{\frac{W_1}{W_1}}\right) \quad (6)$$

3.3 Simulation Results

The simulation of the circuit was done in cadence EDA tool in 180 nm CMOS process by using spectre for schematic analysis and virtuoso for layout analysis at room temperature. For circuit simulation we use the ADE window for different type analysis of the circuit, like DC, AC, Trans, parametric, corner, Monte- Carlo etc. For that circuit I was performed DC analysis for calculation of reference output voltage. AC analysis for calculation of power supply rejection ratio, Noise analysis for calculation of noise density, parametric analysis for showing the effect of different parameters variation on circuit performance.

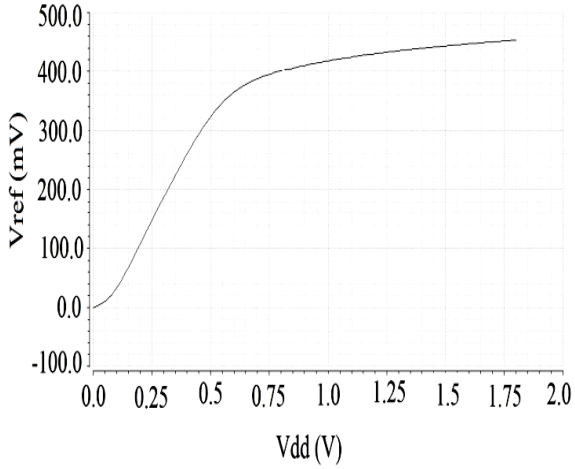

Fig.2. Generated reference Output Voltage as a function of operating Voltage at absolute temperature

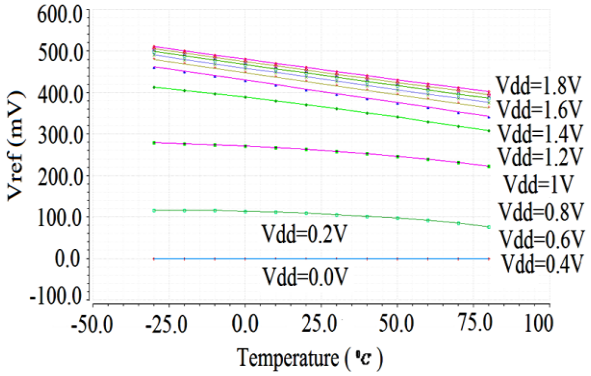

Fig.3. Generated Output Voltage as a variation of temperature at different values of operating Voltage

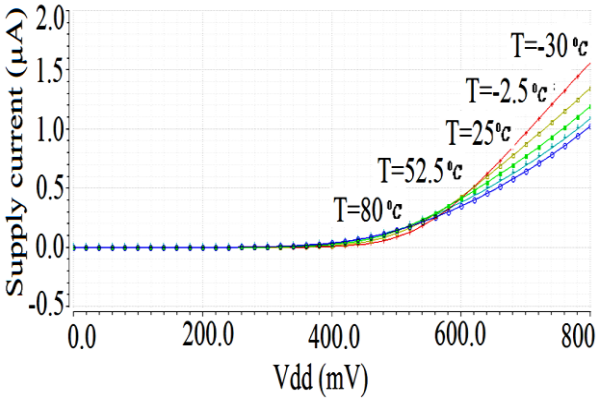

Fig.4. Current flows from the operating Voltage as a variation of operating voltage at different value of the temperature

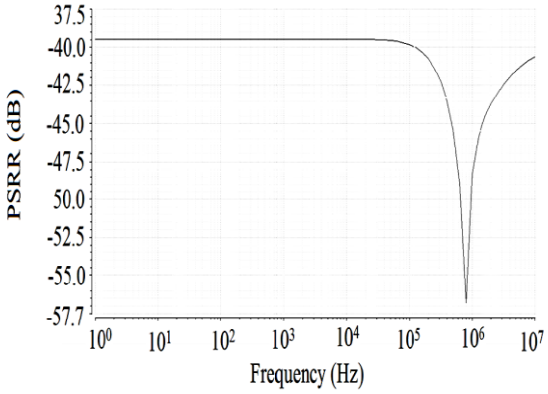

Fig.5. PSRR at absolute temperature for operating voltage of 0.8 V

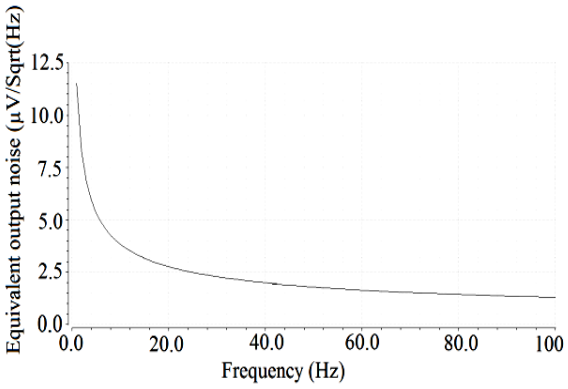

Fig.6. Measured equivalent output noise density ($V/\sqrt{Hz}$) from 1 Hz to 100 Hz

Above shown all simulated result in which fig.2 shows the Reference output voltage (V_{REF}) versus supply voltage (V_{DD}) curve at room temperature. The circuit starts working properly with V_{DD}=0.8 V. in the operating voltage range from 0.8 V to 1.8 V, generated reference voltage was 400mV. In this operating voltage range, output voltage varies by 1.3mV at maximum due to this a supply sensitivity of $0.132\%/V$. The reference Voltage dependence on variation of temperature for different values of the operating voltage is shown in fig.3 The measured temperature coefficient at V_{DD}=0.8 V is $27ppm/$℃ .The current flows from the voltage supply as a function of the supply voltage for different values of the temperature is shown in fig.4.The power supply rejection ratio, without any filtering capacitor, is -39dB at 100 Hz and -40dB at 10MHz,for the smallest supply voltage as shown in fig.5.The measured equivalent output noise amplitude, shown in fig.6. In the frequency range 1Hz to 100Hz, at 100 Hz its value is $1.3\mu V/Sqrt(Hz)$.

4. CONCLUSION

A Nano power voltage generator has implemented in 180 nm CMOS technology. It works with transistors in sub-threshold characteristics and in saturation region, thus allowing a work with two different threshold voltages, which allow a remarkable reduction in the minimum supply voltage and power consumption .The complete suppression of the temperature variation of mobility in a wide temperature range, and the elimination of the body effect .It allow us to achieve a

very small temperature constant of 27 $ppm/℃$ .The minimum operating voltage of only 0.8 V and power consumption 953 nW, which makes the circuit very attractive for low power application.

TABLE: 1 Comparison of Reported low-power CMOS voltage reference circuits

	This work	[6]	[8]	[2]	[5]
Process (µm)	0.18	0.18	0.18	0.35	0.35
$V_{DD}(mV)$	.8-1.8	.45-2	.85-2.5	0.9-4	1.4-3
I_{DD} (µA)	1.2	.007	N.A.	.04	.2143
V_{REF} (mV)	400	263.5	221	670	745
TC $(ppm/℃$	27	142	271	10	7
L.S $\%/V$	0.132	0.440	0.905	0.270	0.002
PSRR @ 100Hz 10MHz (dB)	-39 -40	-45	N.A.	-47 -40	-45
Power (µW)	0.953	.0026	3.3	0.036	0.3

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