



Design and Simulation of Single-electron Tunneling based Nano-electronics Circuits

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ABSTRACT

Among various nanotechnology devices, single-electron tunneling devices are the most promising candidates to substitute the present CMOS devices. In this paper, a new single-electron threshold-logic circuit module is presented for realizing and implementing Nano-electronic circuits. The proposed module can be dedicated to implement all basic logic gates, such as OR, NOR, AND, NAND, XOR and XNOR gates, that can be integrated in various manners to design digital circuits. The simulation results demonstrate the accuracy and stability of proposed circuit module. Design capability and flexibility of this module are further evaluated through the synthesis of high-level circuits.

Keywords

Nanoelectronics, SET technology, Threshold logic, Circuit module.

1. INTRODUCTION

The CMOS technology has seen tremendous growth in the past few decades. The electronic elements scaling aims at growing process speed and decreasing in energy used. The scaling of CMOS devices are continuing to satisfy high performance operation but approaching towards its limiting size. For this issue, the electronic industry is looking for different materials and devices to replace the existing silicon-based CMOS devices to be used in the implementation of circuits. There have been studies signifying that the transistor in CMOS technology cannot shrink beyond a specified extent dictated by the principle of its work [1-3]. These studies have directed to investigation about promising future technologies to increase scaling possibilities such as single-electron tunneling, spin-stabilized magnetic, rapid single-flux-quantum, resonant-tunneling diode and carbon-nanotube devices [4-8].

Nanotechnology deals with the devices implementation at a Nano-scale size that is currently challenging the entire electronic industry in its effort to further decrease the design of integrated circuits. Mastering of technology at this size range has the ability to customize any doable type of materials the way we need. The SET technology is the greatest emerging technology accepted to meet the required features and to replace the current CMOS technology [9-11]. SET based devices and circuits have received enormous attention in the research community. The SET device means the possibility to control the place and transport of an electron based on the quantized nature of charge. The SET circuits have potential advantages of ultra-small size and ultra-low power consumption [12-14]. However, most of nanoelectronic

circuits have been realized as a network of SET-based AND, OR and NOT gates that might be severely affected by a great circuit-depth and alternative solutions are required.

A potential alternative solution is the threshold logic gate (TLG) based design [15-17]. The TLG-SET based circuit design is an emerging area for development of future low power ultra-dense Nano-electronics circuits. A number of research works have been reported regarding the possibilities and advantages of TLG-SET based designs and implementations of useful logic functions [18-21]. On the other hand, reversible logic has attractive perspective of constructing logic circuits that are composed of connected reversible gates to attain almost zero power dissipation [22,23].

The main objective of this work is to present the design and simulation of new Nano-electronic circuit module using SET technology and threshold-logic based approach. This module can be customized to realize basic logic gates in order to utilize it in aspects of digital circuit design.

2. FUNDAMENTALS

2.1 SET Technology

The tunnel junction and transistor are the basic elements of single electron tunneling (SET) technology. In SET technology, the transistor, as shown in Figure 1, contains two SET junctions with two capacitors connected in gates. The junction is characterized by a resistor R_j and a capacitor C_j based on its physical design. The two SET junctions create a quantum island that individual electrons can only arrive to it by tunneling through one of two tunnel junctions. This procedure is based on the tunneling effect and the Coulomb blockade principles of single-electronics [24]. Therefore, the charge of island can be changed by transistor gates to control the phase-shift of Coulomb oscillation as well as the single-electron movement through a junction.

The charge transport through the SET junction is referred to as tunneling, where the single-electron transport through this junction is indicated as the tunnel event [9,25]. Even only single electron tunneling may harvest an e/C voltage across the SET junction, where C is referred to total capacitance and e represents the electron charge (1.602×10^{-19} C). The SET junction has the same definition of PN-junction in the MOSFET whereas the formed island has the same definition of MOSFET channel. Therefore the SET transistor can be used as an electronic switch where it is pushed up into the Coulomb blockade state as an OFF-state or else it can be permitted to follow the current that is considered as the ON-state.

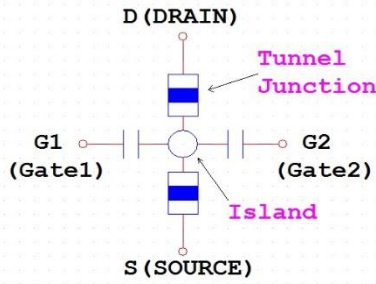


Fig 1: The schematic diagram of single-electron transistor

The need for SET-based circuit simulation has long been recognized [26] and several simulators and simulation methods have been developed to support SET-based circuit design [27-30]. SIMON simulator [28] uses a combination of the Monte Carlo method with direct calculations. The Monte Carlo method is utilized in SECS simulator [29,30] with the free-energy change of simulated circuit to determine the tunnel rating of possible tunnel events, supporting thus an actual time in the simulation of any arbitrary SET-based circuit. In this paper, proposed SET-based circuits are analyzing by both SECS and SIMON single-electronics simulators.

2.2 Threshold Logic

In threshold-logic based approach, the threshold-logic gate (TLG) performs a comparison between the weighted sum of inputs and the threshold value. If the weighted sum of inputs is lower than the threshold, the gate yields logic 0; else, the output is logic 1. The symbol of TLG gate is depicted in Figure 2a. A generic single-electron threshold-logic gate suggested by C. Lageweg et al [9] is illustrated in Figure 2b. The input positive voltages V^p weighted by their input capacitances C^p are added to V_j and the input negative voltages V^n weighted by their input capacitances C^n are subtracted from V_j . The SET junction has the critical voltage V_c that can be adjusted using the bias voltage V_b weighted by C_b and acted as the threshold. The function $F_s(X)$ for this circuit is given by

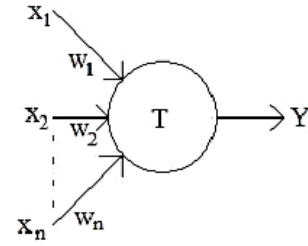
$$F_s(X) = C_\Sigma^n \sum_{k=1}^r C_k^p V_k^p - C_\Sigma^p \sum_{l=1}^s C_l^n V_l^n - T_s \quad (1)$$

$$T_s = 0.5(C_\Sigma^p + C_\Sigma^n)e - C_\Sigma^n C_b V_b \quad (2)$$

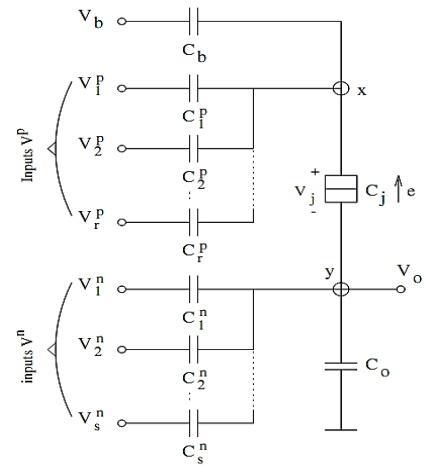
$$C_{\Sigma}^p = C_b + \sum_{k=1}^r C_k^p, C_{\Sigma}^n = C_o + \sum_{l=1}^s C_l^n \quad (3)$$

The TLG-SET gate is used to implement the Boolean function if the circuit parameters are chosen appropriately. The single-electron buffer/inverter should follow any threshold-logic gate to deliver enough driving ability and stability [9,31]. In this paper, input/output signals are assumed correspond with the following voltages: logic 0 = 0V, logic 1 = $0.1e/C$, where C acts as a unit for capacitance. For the circuit simulations, it is assumed that $R_j=100\text{ K}\Omega$ and $C=1\text{ aF}$, resulting in logic 1 = 16 mV. For the buffer/inverter, the circuit parameters are used as in [9]. In this paper, the following circuit parameters are used in the design of threshold gates: $V_b=16\text{ mV}$, $C_j=0.1C$, $C_o=9C$, and $C^p=C^n=0.5C$. C_b is the variable parameter of threshold gate that is

determined depending on the specific expression of designed gate.



(a)



(b)

Fig 2: TLG gate: (a) symbol, (b) n-input TLG-SET based structure

3. PROPOSED BASIC LOGIC MODULE

In this section, the basic logic module (BLM) is proposed as a universal logic circuit that can represent all basic logic gates. It is implemented using single electron tunneling (SET) technology based threshold logic gate (TLG) approach.

The proposed BLM circuit is implemented as a single 2-to-1 multiplexing circuit as shown in Figure 3a. It is constructed from two AND gates in the first level with A , $I0$ and $I1$ as inputs while their outputs $G0$ and $G1$ are as inputs of OR gate in the second level with F as an output. The proposed TLG based BLM diagram is shown in Figure 3b. It can be realized using three buffered threshold logic gates; TLG0, AND, and OR gates. The threshold logic equations for the outputs of these gates can be written as

$$G0 = sgn\{A - I0 + 0.5\} \quad (4)$$

$$G1 = \text{sgn}\{-A - I1 + 1.5\} \quad (5)$$

$$F = \text{sgn}\{-G0 - G1 + 0.5\} \quad (6)$$

The circuit schematic of proposed BLM is shown in Figure 3c. The circuit parameters of TLG-SET structure are: $C_b = 11.7C$ (TLG0), $C_b = 12.25C$ (AND), and $C_b = 10.6C$ (OR). The proposed BLM can be dedicated to realize all basic logic gates by selecting proper inputs $\{I0 \text{ and } I1\}$ as listed in Table 1. All the possible combination of the inputs $\{A, B\}$ used for the simulation are shown in Figure 4, where the voltage levels $\{0 \text{ mV and } 16 \text{ mV}\}$. The presence of positive charge (that is one electron missing) on the output nodes corresponds to logic 1, whereas no charge corresponds to logic 0.

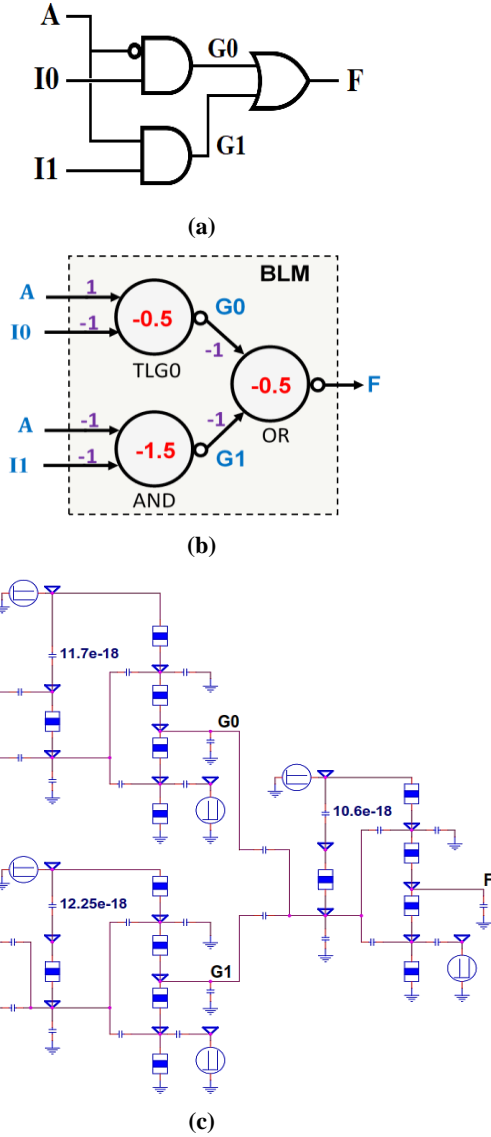


Fig 3: Basic logic module (BLM): (a) logic diagram, (b) TLG representation, (c) TLG-SET structure

Table 1. Basic modes of BLM

Mode	Control Pins		$F(A,B)$	Basic Gate
	$I0$	$I1$		
1	B	1	$A + B$	OR
2	\bar{B}	0	$\bar{A} + \bar{B}$	NOR
3	0	B	AB	AND
4	1	\bar{B}	$\bar{A}\bar{B}$	NAND
5	B	\bar{B}	$A \oplus B$	XOR
6	\bar{B}	B	$A \odot B$	XNOR

The output signals of simulated BLM-based logic gates are also depicted in Figure 4. The simulation results represent six modes of BLM (Table 1) that are OR(A,B), NOR(A,B),

AND(A,B), NAND(A,B), XOR(A,B), and XNOR(A,B) results, respectively. The results obtained from the simulation are found to be satisfactory.

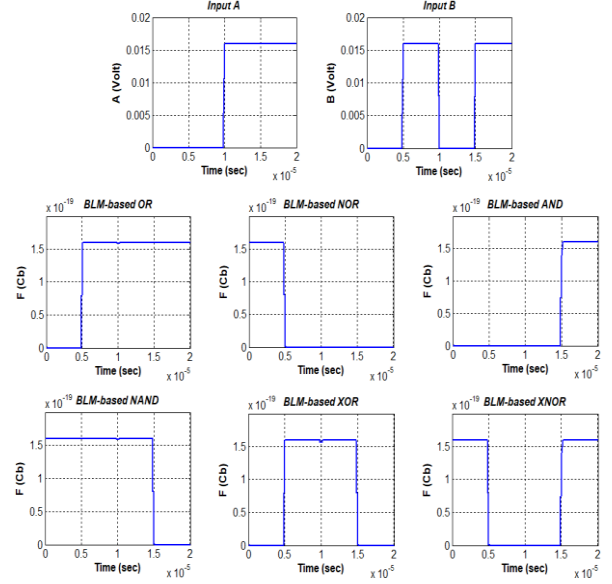


Fig 4: Input and Output waveforms of dedicated BLM circuits

The Boolean function Y is introduced in Eq. 7 as an example for logic circuit implementation using the proposed module. The implementation of logic function Y based on BLM is given in Figure 5a. The blocks of BLM1, BLM2 and BLM3 are dedicated as AND, XOR and OR gates, respectively. The complete TLG-SET schematic of designed circuit is shown in Figure 5b. The simulation result is shown in Figure 5c for Boolean function Y in respect to all possible input combinations, the correct output is generated. Consequently, the proposed module is a single-electron tunneling universal circuit that can be utilized to implement Boolean logic functions without needing to change its structure or parameters of TLG-SET based design.

$$Y = A.B + A.\bar{C} + \bar{A}.C \quad (7)$$

4. CONCLUSIONS

This paper introduces a new circuit module that can be used in the design and development of Nano-electronic circuits using single-electron tunneling (SET) technology based threshold-logic gate (TLG) approach. The proposed basic-logic-module (BLM) has been used as the universal gate for implementing all basic logic gates that can be utilized in the synthesis of logic circuits. The performance of proposed circuit module has been verified through SET simulations, and all results have been found to be satisfactory. Moreover, it has been shown that the proposed single-electron threshold-logic building block can be configured to implement efficient high-level circuits. Consequently, the proposed module is a good candidate to build and develop TLG-SET based Nano-electronic circuits without needing to change design parameters.

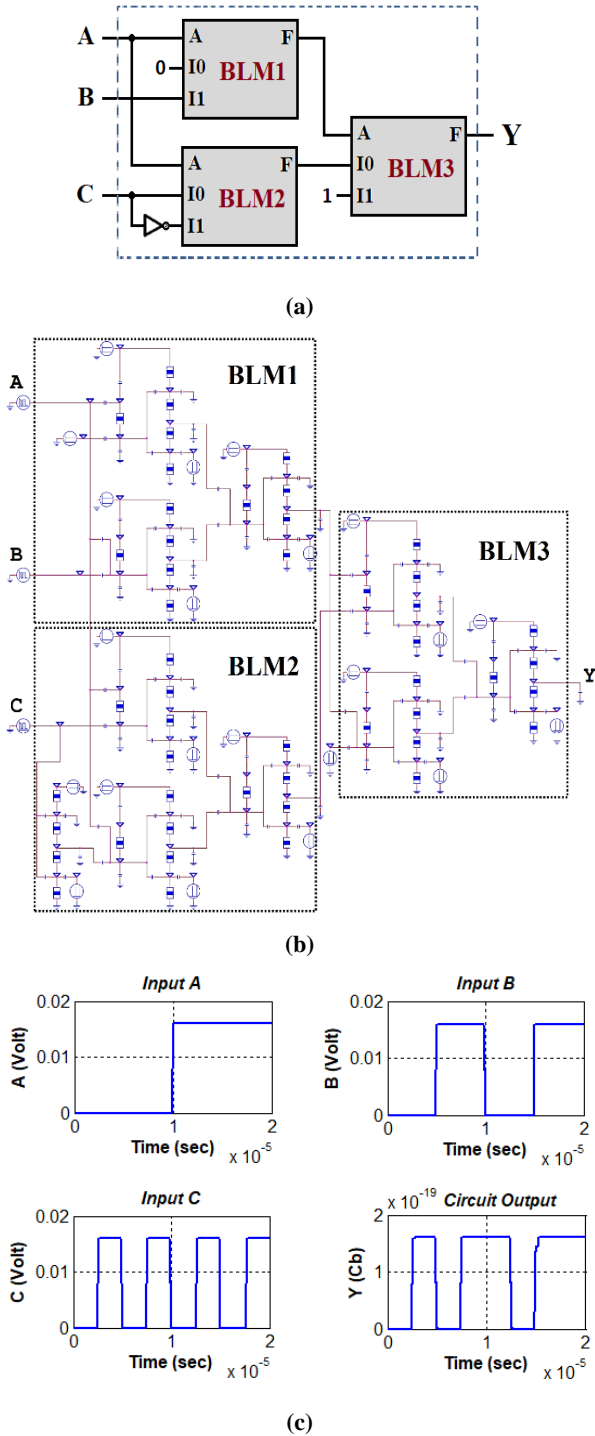


Fig 5: BLM-based circuit of Y function: (a) block diagram, (b) TLG-SET layout, and (c) simulation result

5. ACKNOWLEDGEMENTS

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