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Reduction Technique for Power Leakage in Complementary Metal Oxide Semiconductor Circuit using Deep Submicron Technology

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ABSTRACT
Leakage power reduction has become a major factor in all modern electronic hand held and portable devices due to advancement in the scaling of all Complimentary metal oxide semiconductor devices and circuits. For the reduction of power leakage in the circuit we have used a technique to reduce leakage power at various gates. The approach used here is stack with pass transistor for reduction of leakage power in various gates in the circuit. A parallel combination of NMOS and PMOS transistor is used in parallel for enabling stacking of the transistor for leakage reduction in pull up and pull down network of the transistor. In pull up network NMOS transistor is inserted in parallel to PMOS sacked transistor to maintain Logic level 1. NMOS transistor gets connected to V_{dd} in pull up Network in sleep mode then pass transistor cut off which achieves a reduction of leakage of 44.63%, 44.63%, 87.02 and 87.44% at 25 Celsius as calculated in two input NAND gate. Also there is a reduction in the Average dynamic power as 15.24%, 15.28%, 35.20%, 31.20% respectively. Area, Delay and Power requirement is satisfied by choosing particular variant of NAND gate. Hence, a trade off is made among these parameters. This technique is also implemented in One bit Full Adder for Low Power leakage design of the circuit.

Keywords
Low Power Design, Leakage reduction, Integrated Circuits, VLSI.

1. INTRODUCTION
Most widely used approach for VLSI (Very large scale circuit) circuit design used today is CMOS (Complementary Metal Oxide Semiconductor). It has completely replaced the approaches used like nMOS process or Bipolar transistors for designing Digital circuits and systems. Customer choices are changing rapidly with the increase in popularity of digital and hand held devices. All devices like Mobile, Kindle, Smart watch, tablet are part of a comfortable and luxurious life. Previously, a system is used to driven by the its performance and operational speed but as the trend have changed and now the preference is now shifted to the devices which are compact, high end performance, low power consumption and portable. CMOS Circuits choices decide the performance responsible for the power consumption of the device. A range of topologies are used for the implementation of multiple Arithmetic and Logical units and functions. With the advancement in the chip manufacturing industry, to accommodate maximum possible transistor in each die with Improvement in the performance of chip operation in the CMOS technology. This has led immense competition in the semiconductor industry forcing manufactures to increase number of transistors in each single chip for the cost reduction. The demand is increasing exponentially which has also resulted in the form of increased power dissipation. Increase in the amount of power consumption is one of the dominating factor for chip manufactures, as it results in the form of high temperature of the chip reducing the battery life of the devices and thus, reducing life of battery. In order to achieve high performance and higher driven capability at a lower voltage, V_{TH} is lowered. As the value of Threshold Voltage (V_{TH}) is reduced there is a increase in the Sub threshold Leakage Current (I_{SUB}). As there is a proportional relationship between VTH and ISUB in nanoscale. It is essential to make use of advanced leakage reduction techniques in nanoscale.

However, most effective and high performance technique for designing of VLSI circuits is CMOS design technique. As the latest electronics system are developed either wireless or wired they are consistently challenge the limitation of CMOS technology in various fronts. To overcome these design issues it is essential to go for devices with low power consumption and less power dissipation or leakage during the idle mode of operation and then to increase the life of the battery.

When the transistor came into the existence in the initial period the main focus was to improve the performance and reduce the size of the system but not on power dissipation. But as the advancement took place in the modern world it is most important to design the portable systems with low power consumption and low power leakage. As there is huge demand of portable devices with the advent of mobile phone it is essential to limit power dissipation and design low power devices. Battery operated devices such as calculators, pacemaker, digital medical equipment and portable military equipment is given by modern low power electronics. The research work focus on finding the circuit with low power at circuit or at the transistor level of operation in the digital circuit design. Thus multiple circuit style techniques are used from traditional till the current advanced processing techniques. Research findings with their merits and demerits for all type of techniques is discussed in this literature review,

2. BACKGROUND
Deep Sub Micron (DSM) technology as in this technique large number of gates are accommodated in to a single integrated chip, with smaller dimensions. As a result of large number of gates in the single chip the power densities is increased rapidly also total power consumption is increased significantly. It is important to design low power circuit in present scenario. However with the reduction of power dissipation there is a tradeoff in the timing and area of chip at various stages of the design implementation. Designers needs to engineer accurate

and effective models to perform successful and efficiently adjustments in these tradeoffs. These issues can be handled efficiently by understanding various types of designs and there role in power dissipation in nanoscale of various digital circuits. CMOS(Complementary metal oxide semiconductor) technology is chosen as it is the most prominent digital Integrated Circuit implementation technology. Here most effective and low power leakage techniques are discussed for handling power dissipation. Also digital circuits are designed with one bit, four bit and four bit adder subtraction adder are designed which consume minimum power in the standby mode of operation.

3. LITERATURE REVIEW

Milena Djukanovic et. al., [1] 2011, Effectiveness of Leakage Power Analysis (LPA) attacks cryptographic in the presence of process variations. Reference circuits were designed using logic styles evaluated for the simulations of 65 nanometer. Process variations of the Leakage Power Analysis attacks. Result shows Leakage Power Analysis attack are rather useful in die to die and with in die process technology. Different logic style comparison shows that in case of CMOS(Complimentary Metal oxide Semiconductor) logic circuits are vulnerable to Leakage Power Analysis attack. Different logic style which are robust when compared with the traditional Differential Power Analysis (DPA) attacks. Surprisingly, analysis also shows that logical styles are more vulnerable to the Leakage Power attacks. Leakage Power attacks are more dangerous to the smart card security compared with the Differential power attacks.

Afshin Abdollahi et. al.[13] 2004, This research work describe two runtime operations for the reduction of CMOS leakage current. In both the cases, it is to be noted that system releases a "sleep" signal for indicating circuit operating in the standby mode of operation. Here, the "sleep" signal is shifted to new set external input, Thus, internal signals are pre-selected in the circuit for setting up the logic values all internal signal in order to reduce leakage current of circuit. Minimization of leakage current is done due to the reason of CMOS gate dependency on the input applied. The other method used for the reduction of CMOS leakage current involves addition of some of the gates to the nMOS and pMOS transistor to obtain control over internal signal of the digital circuit and reduction in the leakage current of the gate by the use of stack effect.

M Alioto et. al.[13] 2004, This work presents a model in multibit Power Analysis which attacks buses, with focus on cryptographic design algorithm. The analysis gives deeper insight on of the DPA with various parameters that define the attack, the algorithm the processor architecture which is responsible for the implementation of this design. Here, the practical DPA is given by main parameters responsible for attack in analytical approximations, thus a figure of merit for measurement of DPA of multibit attack is implemented. Figure of merit is responsible for identification in order to maximize the effective attack of DPA i.e. in the given condition under a cryptographic chip must be made test for robustness measurement. This model is used in DES and AES algorithm while both simulations are completed on MIPS32 design architecture on a FPGA implementation. The accuracy of the model is found to be adequate, but the resulting error is always less than 10 percent and very few number of points.

L Lin at. al. [7]2008, Vulnerability for crypto system in power analysis for DPA attacks thus counter measurement have been concluded. With the scalability of supply voltage of CMOS technology below 90 nanometer, power leakage with a increasing role in dissipation of power. Further, digital crypto systems need for the current trend, though it is not important in low cost crypto systems with smart cards and RFED tags. In this research work, we propose the impact of leakage power dissipation in conventional novel DPA.

We explore the use SPICE simulation for exploration of the leakage dependence on the pattern of input of various logic gate implemented in 65 nanometer, 90 nanometer, and 45 nanometer CMOS technology. We now go for the simulation of LDPA on a subset of DES crypto system with 120 round, in contrast with the 200 rounds reported for a DPA in 180 nanometer technology. Here demonstration of a DES implementation is done by the use of DPA resist logical style with the broken LDPA in 2000 around rounds, when compared with DPA using minimum 5000 rounds.

K Tiri at. al. [13] 2004, Here the research work gives a design approach for the implementation of a advanced DPA secured resistant crypto processor. This method adopted is suitable for the integration of automated standard cell using FPGA or ASIC. Power consumption is almost constant with the help of new compound standard cells using technique which combines with the standard building blocks for making new cells. With the experimental results it is found that there is a 50 times reduction in power consumption.

4. STACK APPROACH

A very famous approach used for the purpose of leakage power reduction is the stack approach that is responsible for the breaking down of the existing transistor into two equal size. Threshold voltage and the sub threshold leakage current are having a exponential relationship due to the body effect. It is evident from these two facts that a reduction in the value if sub threshold leakage in the device is done with the combination of two or more transistors. All the transistors above the lowest transistor have a experience of the increase value of threshold voltage for the reason that the souce and body voltage variation is shown in the figure. But there is a strong detoriation in the technique.

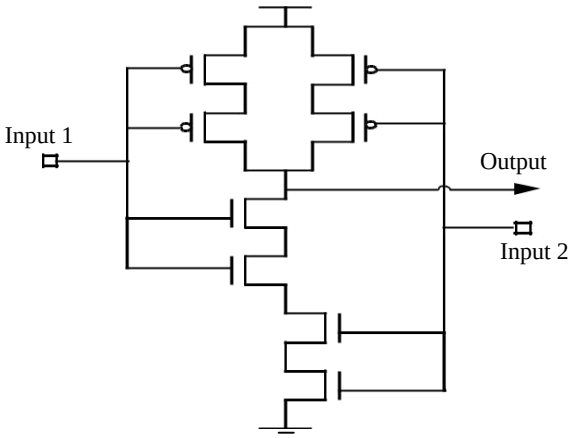

Fig.1. Stack Approach Based Two Input NAND Gate

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5. SLEEPY STACK APPROACH

This technique is used for the purpose of dividing the with the level maintaining of the ratio of W/L in the original design of the transistor. We make a insertion of the transistor in the sleep mode of operation with the parallel stack. A combination of the two method is done with the division of the existing transistor without having a effect on the capacitance of the given circuit. When the circuit is in the state of operation the PMOS transistor S is zero and NMOS *S'*=1, in this condition all the sleep transistors are made in ON state. Even when there are ON resistance of the power switching is much more than that of the OFF resistance. It is still responsible for the creation of a small voltage at node. Driving capabilities are reduced due to the reduction in the value of the voltage and the threshold voltage of the NMOS transistor circuit design.

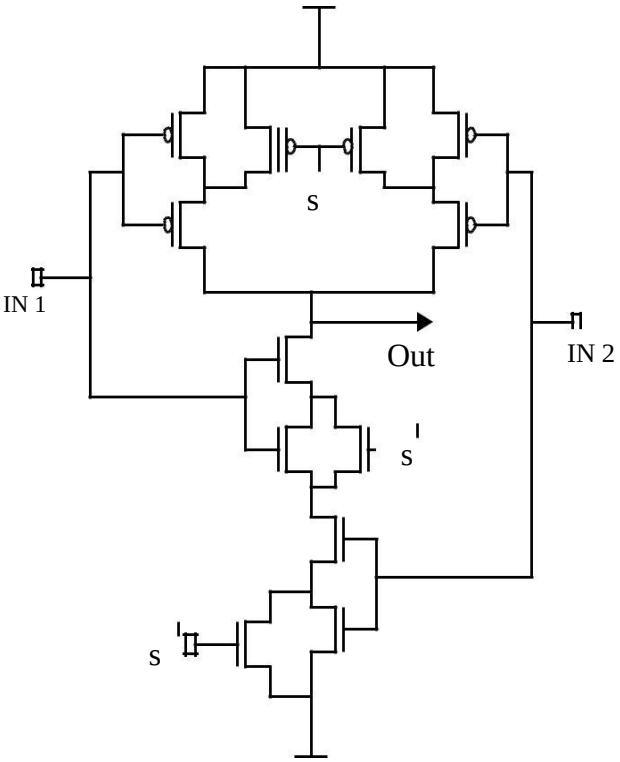

Fig.2 Sleepy Stack Approach Based Two Input NAND Gate

Other techniques like Power gating (MTCMOS) and SCCMOS are technology dependent, thus they need a modification in technology. MTCMOS have a reduction the level of the leakage but correspondingly increase the value of the propagation delay. There is a requirement of a additional bias generator in the SCCMOS. It is responsible for the overdriving and the gate terminal of the PMOS and the NMOS circuit design in the sleep transistor. There is a another leakage reduction technique in the runtime with a association of the controller circuit in the PMOS and NMOS. Here there is a additional requirement of the DC supply voltages.

6. IMPLEMENTED DESIGN

Structure used for the operational analysis of the proposed lowleakage power design circuit used with stack in pass transistor logic. The circuit proposed here is impressive for comparison with previously known approaches, i.e., Conventional logic Gates. In over the implemented approach the circuit we are using here have to be introduced by two technique for stack approach with the use of pass transistor approach for reduction in the level of leakage power consumption for implementation in the circuit. Here a combination of two NMOS pass transistor is used for the placement below pull up network circuit and PMOS transistor placed in paralleled form to the NMOS transistor logic in between pull up network circuit and pull down network unit. In case of Pull up transistor Turn the ON condition of the NMOS pass transistor logic and in case of the Pull down transistor turns the ON mode of the PMOS pass transistor in the active mode of operation of the CMOS design circuit, during the sleep mode of operation both the pass transistor turns condition changes to OFF state and rail the CMOS network from the supply voltage which help for the reduction in the leakage power of the transistor of the CMOS circuit. Similar action can be taken for the repeating of the pull down network of the design while with the involvement in the interchanging of pass transistors in the NMOS transistor gives advantage of providing the stacking effect inorder to maintain the value 0 in the sleep mode of the operation and PMOS pass transistor connecting in the parallel for the NMOS transistor logic of operation. For maintaining an output voltage value to be 0 in the PMOS logic transistor Ground is connected sleep mode of operation.In order to achieve Logic in the proper form at the output of the NMOS transistor circuit we use to keep connected PMOS transistor to Vdd to GND. Here it is also to be noted that the stacking in transistor is responsible for the reduction of the leakage power in implemented approach of operation. Thus, for maintaining the proper higher logic we here insert a NMOS transistor logic in parallel combination to PMOS stacking transistor in the pull up mode of network operation, Here we connect a sleep transistor to the Vdd of the design for the pull up network. In this sleep mode of operation, these NMOS transistors connects with the Vdd in the pull up network and sleep transistor in the cut off mode of the operation.

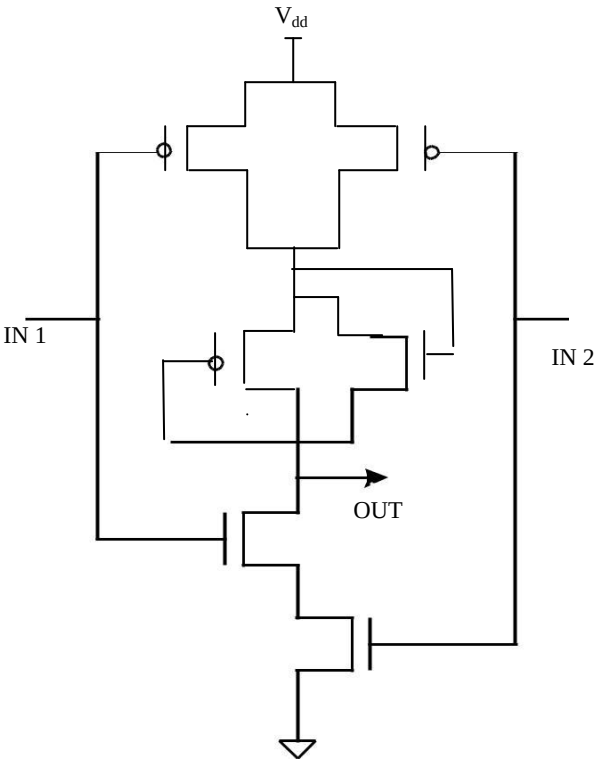

Fig.3. Implemented Circuit Design

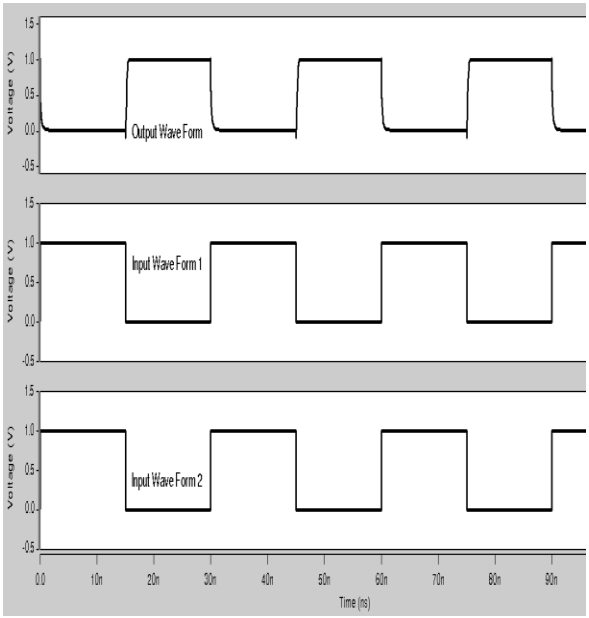

Fig.4. Output Wave form of Proposed Circuit

7. SIMULATION RESULT

Table I. Dynamic Power at 45nm 25^{0}C

Gates	Average Power(μW)	Delay(pS)			PDP
		T_R	T_F	$T_R+T_F=T_{Total}$	
NOT	0.2057	4.847	5.181	5.014	1.031
AND	0.4163	10.96	5.424	8.192	3.410
NAND	0.2627	8.455	3.352	5.903	1.550
NOR	0.2336	9.279	3.094	6.186	1.445
EXOR	0.3595	6.247	6.572	6.409	2.304

Table II. Dynamic Power at 45nm 100^{0}C

Gates	Average Power(μW)	Delay(pS)			PDP
		T_R	T_F	$T_R+T_F=T_{Total}$	
NOT	0.3048	4.671	5.418	5.044	1.537
AND	0.6534	11.21	5.318	8.264	5.399
NAND	0.3901	8.374	2.779	5.576	2.175
NOR	0.3205	9.810	3.173	6.491	2.080
EXOR	0.4065	6.046	6.874	6.362	2.586

Table III. Dynamic Power at 32nm 25^{0}C

Gates	Average Power(μW)	Delay(pS)			PDP
		T_R	T_F	$T_R+T_F=T_{Total}$	
NOT	0.1440	5.382	5.612	5.497	0.791
AND	0.2708	11.19	5.658	8.424	2.281
NAND	0.1862	9.422	2.694	6.058	1.127
NOR	0.1661	10.73	3.571	7.150	1.187
EXOR	0.1875	11.96	12.83	12.39	2.323

Table IV. Dynamic Power at 32nm 100^{0}C

Gates	Average Power(μW)	Delay(pS)			PDP
		T_R	T_F	$T_R+T_F=T_{Total}$	
NOT	0.2210	5.117	5.810	5.463	1.207
AND	0.4534	11.15	5.940	8.545	3.874
NAND	0.2860	9.604	3.053	6.328	1.809
NOR	0.2328	11.06	3.235	7.148	1.664
EXOR	0.2865	10.93	11.58	11.25	3.223

Table V. Leakage Power Consumption at 45nm at 25^0 C

Gates	Leakage Power Consumption at 45nm			
	00	01	10	11
NOT	21.83	75.23		
AND	60.45	109.1	76.07	172.8
NAND	31.46	149.8	103.6	150.4
NOR	43.63	83.11	72.86	111.8
EXOR	155.9	108.4	108.4	155.9

Table VI. Leakage Power Consumption at 45nm at 100^0 C

Gates	Leakage Power Consumption at 45nm			
	00	01	10	11
NOT	52.00	83.32		
AND	119.3	188.6	152.2	218.9
NAND	39.88	260.2	154.34	166.5
NOR	103.8	95.12	80.98	114.8
EXOR	176.0	166.5	166.5	176.0

Table VII. Leakage Power Consumption at 32nm at 25^0 C

Gates	Leakage Power Consumption at 32nm			
	00	01	10	11
NOT	10.14	24.88		
AND	21.34	48.66	30.00	59.92
NAND	3.921	31.21	12.57	49.73
NOR	20.26	24.97	24.33	42.90
EXOR	49.28	43.70	43.70	49.28

Table VIII. Leakage Power Consumption at 32nm at 100C

Gates	Leakage Power Consumption at 32nm			
	00	01	10	11
NOT	73.87	44.98		
AND	116.1	185.1	163.9	164.4
NAND	28.07	96.31	75.11	89.80
NOR	146.8	44.88	42.66	51.24
EXOR	87.44	170.98	170.98	87.44

Table IX. Implemented Dynamic Power at 45nm 25^{0}C

Gates	Average Power(μW)	Delay(pS)			PDP
		T_R	T_F	$T_R+T_F=$	
NOT	0.1727	1.912	6.525	4.218	0.728
AND	0.4039	6.271	5.838	6.054	2.445
NAND	0.2373	7.560	6.466	7.013	1.664
NOR	0.2143	1.183	11.76	6.471	1.386
EXOR	0.2831	2.953	14.09	8.521	2.412

Table X. Implemented Dynamic Power at 45nm 100^{0}C

Gates	Average Power(μW)	Delay(pS)			PDP
		T_R	T_F	$T_R+T_F=T_T$	
NOT	0.2628	1.794	6.555	4.175	1.097
AND	0.6191	6.614	5.614	6.114	3.785
NAND	0.3566	7.167	6.541	6.854	2.444
NOR	0.3010	0.958	12.01	6.484	1.951
EXOR	0.3464	2.255	15.03	8.642	2.993

Table XI. Implemented Dynamic Power at 32nm 25^{0}C

Gates	Average Power(μW)	Delay(pS)			PDP
		T_R	T_F	$T_R+T_F=T_{Total}$	
NOT	0.1255	3.701	14.00	8.850	0.464
AND	0.2612	5.762	5.215	5.488	1.433
NAND	0.1611	3.901	5.440	4.670	0.752
NOR	0.1286	1.144	19.28	10.21	1.313
EXOR	0.1345	7.322	22.91	15.11	2.032

Table XII. Implemented Dynamic Power at 32nm 100^{0}C

Gates	Average Power(μW)	Delay(pS)			PDP
		T_R	T_F	$T_R+T_F=T_{Total}$	
NOT	0.1403	3.555	14.20	8.877	1.245
AND	0.4235	5.711	5.732	5.721	2.422
NAND	0.2460	3.988	5.343	4.665	1.147
NOR	0.1839	0.869	18.88	9.874	1.815
EXOR	0.1956	9.961	29.61	19.78	3.868

Table XIII. Implemented Leakage Power Consumption at 45nm at 25^0 C

Gates	Leakage Power Consumption at 45nm			
	00	01	10	11
NOT	13.74	39.04		
AND	55.35	84.65	64.56	90.69
NAND	19.65	42.59	23.43	76.94
NOR	27.05	46.08	38.38	59.70
EXOR	77.06	57.62	57.62	77.06

Table XIV. Implemented Leakage Power Consumption at 45nm at 100^0 C

Gates	Leakage Power Consumption at 45nm			
	00	01	10	11
NOT	35.60	47.32		
AND	103.5	170.0	148.6	129.1
NAND	26.28	64.64	44.74	93.31
NOR	69.20	55.88	46.49	63.48
EXOR	94.28	92.74	92.74	94.28

Table XV. Implemented Leakage Power Consumption at 32nm at 25^0 C

Gates	Leakage Power Consumption at 32nm			
	00	01	10	11
NOT	0.598	13.24		
AND	18.74	37.98	28.50	33.14
NAND	2.788	17.40	8.311	26.30
NOR	12.89	12.00	12.98	21.60
EXOR	25.32	23.34	23.34	25.32

Table XVI. Implemented Leakage Power Consumption at 32nm at 100^0 C

Gates	Leakage Power Consumption (nW)			
	00	01	10	11
NOT	3.023	15.66		
AND	103.7	170.7	159.9	112.2
NAND	23.42	66.59	56.64	56.19
NOR	15.03	20.34	27.08	26.67
EXOR	52.13	108.4	108.4	52.13

A comprehensive performance analysis is made for all the parameters present in the circuit analysis. Here a comparison is made between the implemented circuit design and basic circuit design by using the technique already available and the waveform. The implementation of the design done with this technique for the leakage current reduction with the help of the all the parameters present. This implemented design technique briefs a reduction in the value of leakage current and also the other parameters of the designed circuit. There are parameters in the applied design such as V1 and V2 which are responsible for the reduction of the average delay by a percentage of 14.01%This implemented design gives a cost effective and low power design which operates at a lower voltage level with the good speed of operation.

8. CONCLUSION

This work is focused on the leakage current reduction with the analysis made on the consumption of the power with the help of technology called Deep Submicron technology. Here out main focus in the implementation is to present a novel approach using a ciruit to make a improvement in the swing levels. The associated advantages with the CPL is that they have high level of the functional design with possible minimization in the number of CMOS transistor and the input capacitances. These associated advantages are practically not done due to reason that CPL make use of the additional swing restoration design of the circuit with the use of dual-rail encryption for complete performance improvement. This give a overhead of the unrequired wiring and dissipation in the power. There is a Trade–off to be done for obtaining the required variant of the circuit using area, Delay and Power consumption. There is a Standby current which is a significant portion in the complete power consumption, this upfront a challenge for the designers to make critical factor in low power circuits. It can be concluded that the static power consumption is to be considered always in every design flow.

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