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A 3-Bit 10-MSps Low Power CMOS Flash ADC

Andrew Selasi Agbemenu
Dept. of Computer Eng.
KNUST
Kumasi, Ghana

Ernest Ofosu Addo
Dept. of Info. Eng. and Math.
University of Siena
Siena, Italy

Benjamin Kommey
Dept. of Computer Eng.
KNUST
Kumasi, Ghana

ABSTRACT

Flash ADCs employ multiple comparator circuits to introduce parallelism in data conversion. Having their speed limited only by transistor gate and comparator propagation delay, flash converters have the fastest signal conversion speeds amongst all ADC architecture implementations. This paper details the design of a low power 3-bit flash ADC with a 3V supply realised in 0.6 micron CMOS technology. The designed ADC exhibits a voltage resolution of 34.13 mV and draws 23.88 mW power at 2.17 MHz.

General Terms

Flash ADC, CMOS

Keywords

Resistive ladder, Comparators, Bubble noise suppression, Hysteresis

1. INTRODUCTION

Applications of flash ADCs are widespread in the areas ranging from satellite communication to radar processing where large bandwidth is essential for optimum system operation[7, 6]. The fast nature of these ADCs arise from the parallel comparison of input signals and the high input time quantization speed. This sampling speed is typically limited only by comparators and the digital logic switching. The fundamental performance of these converters is however heavily dependent on the characteristics of their comparators and voltage ladders. Errors in these constituent blocks consequently have severe effects on conversion properties and abilities. With 2^{n-1} comparators, 2^n resistors, and other logic circuits required in a typical n-bit flash converter for operation, these ADCs are naturally plagued with large power and area liabilities.
Flash converters are also limited to low resolutions as the hardware needed, doubles per resolution increase. Power dissipation in this case also increases by more than a factor of two [9, 7]. Non-idealities in converter building blocks can therefore not be tolerated and must be reduced as much as possible. This work explores the use of hysteresis and other techniques in the design of the constituting blocks of a flash ADC to address common converter error sources such as metastability, bubble error, and substrate noise.
This paper is organized as follows. Section 2 discusses the flash architecture, Section 3 discusses the proposed design. Section 4 presents the post layout results and concludes with Section 5.

2. FLASH CONVERTER ARCHITECTURE

The highest potential sample rate characteristic of the flash ADC arises from the rather parallel fashion in which a single analog input signal, V_{IN} is compared to the converter's reference levels to decide correct quantization levels[6] . The 7 reference levels, shown in Figure 1, are typically generated through a resistor ladder where 8 equally valued resistors divide the ADC's applied reference voltage,V_{REF}. Seven comparators are then used to establish a comparison between the input signal and potentials at various tapping points of the voltage ladder established by the resistor string. Each comparator generates a '1' if V_{IN} is larger than its associated reference level and a '0' if otherwise. The combined outputs of the comparators constitute a thermometer code, each of which represents a quantization level. An encoder then used to convert the thermometer code to a 3-bit digital output word. Encoder blocks have been implemented in several different ways. There are implementations such as the multiplexer based encoder [2], fat tree encoder, [8], and ROM encoder[5, 1]. The encoder scheme adopted this design was aimed at efficient code conversion, reduction of errors arising from metastability and also low power budget compliance.

Table 1. : Design parameters of proposed flash ADC

Parameter	Description
Bandwidth	2 MHz
Comparator propagation delay	3.2 ns
Voltage resolution	35 mV
ADC power consumption	30 mW

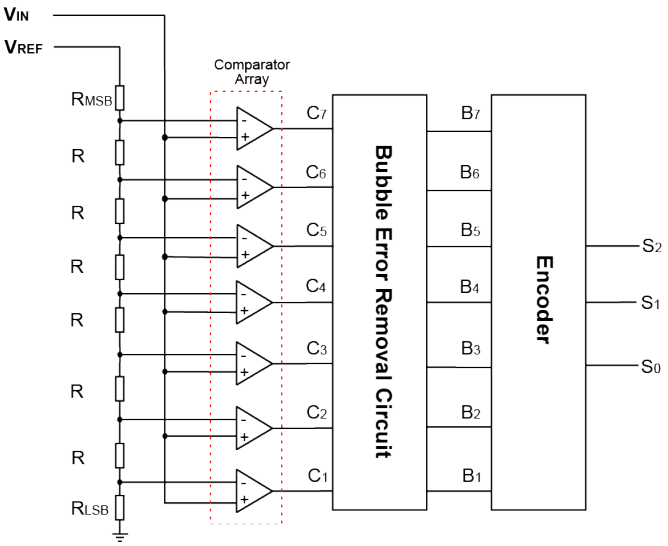


Fig. 1: Architecture of Flash ADC

Table 1 shows the design specification for the proposed ADC.
The operation of ADCs typically involves the approximation of an analog input signal with a corresponding analog output in order to achieve conversion of the signal to a digital word. These approximations results in several errors like the quantization error. For low resolution converters, there exists a strong correlation between the input signal and the quantization noise. Apart from the quantization error, static noise like the deviation of actual quantization levels from ideal levels exist in non-ideal

analog-to-digital converters. These result in both linear as well as non-linear deviations in the transfer curve of ADCs with offset and gain error being typical quantifications of linear deviations. Comparators switch instantaneously when their two inputs, V^+ and V^- achieve equal potential. This behaviour is however altered with the presence of offset voltage, V_{OS}. Outputs of non-ideal comparators therefore experience state switches under the following conditions:

$$V_O = 1 \quad when \quad V^+ > V^- + V_{OS} \tag{1}$$

$$V_O = 0 \quad when \quad V^+ < V^- + V_{OS} \tag{2}$$

Flash ADCs which have their reference voltage levels generated through resistive ladder typically use equal valued resistors for this purpose. The accuracy of quantization levels in this case relies on the degree of matching of the resistors in the string. The comparator voltage input on the j_{th} tap of the resistor ladder is the sum of an ideal voltage term and another consisting of the product of the converter's quantization step and the aggregate of resistor mismatch ratios. Mathematically, the j_{th} voltage tap is given as:

$$V_j = V_{j,ideal} + \frac{V_{REF}}{2^N}.\sum_{k=1}^{j}\frac{\Delta R_k}{R} \tag{3}$$

The ideal voltage term, $V_{j,ideal}$ represents the voltage that would be measured at the j_{th} tap should no resistors deviate from their nominal values, R whiles ΔR_k represents the resistance mismatch error value. From Equation 3, it is evident that the sum of the ΔR_k terms influences the magnitude of each voltage at tap and the converter linearity substantially. The integral non-linearity, INL, which defines the linearity of the comparator's overall transfer curve can therefore be estimated using Equation 4. The effects of resistor mismatches are also evident in alterations in the switching point of the comparators. Equation 5 estimates the switching voltage of the converter's j_{th} comparator.

$$INL = V_{os,j} + \frac{V_{REF}}{2^N}\sum_{k=1}^{j}\frac{\Delta R_k}{R} \tag{4}$$

$$V_{sw,j} = V_j + V_{os,j} \tag{5}$$

3. COMPONENT DESIGN

3.1 Comparator design

The comparator circuit as shown in Figure 2 has three stages: an input preamplifier, a positive feedback and an output buffer. The preamplifier stage improves the comparator sensitivity by boosting weak input signals and shielding the comparator from kickback noise generated by the comparator's positive feedback stage. A fully differential transconductance amplifier with active PMOS loads M_3 and M_4, forms the input stage of the comparator. M_1 and M_2 are sized such that the resulting input node impedance is low in order to facilitate high bandwidth operations. The fully differential nature of the output of the first stage ensured that there was optimum rejection of common mode components of input signals. By choosing a suitable aspect ratio of the current mirrors, M_5 and M_6, these transistors upon acting on the first stage output signal, imparts a current gain. The drain currents, I_X and I_Y are related to the preamplifier's input voltages by

$$I_X = \frac{g_m}{2}(V^+ - V^-) + I_{SS} = I_{SS} - I_Y \tag{6}$$

The comparator's decision making circuit was implemented using positive feedback because this configuration has the capability to distinguish mV-level signals. Noise from sources such as the interfacing digital circuit as well as ADC's power supply were reduced in the feedback circuit by the addition of some amount of hysteresis. Assuming I_X is much larger than I_Y such that transistorsM_7 and M_9 were on whilst M_9, M_10 were off, V_Y is approximately 0V and the value of V_X is determined by Equation 7 where $\beta_A = \beta_7 = \beta_{10}$.

$$V_X = \sqrt{\frac{2I_X}{\beta_A}} + V_{THN} \tag{7}$$

An increase and corresponding decrease of I_Y and I_X values respectively raises the gate overdrive potential of M_{10}, V_{OV10} to 0V; a condition which commences switching. Further changes in the currents in similar fashion causes V_{OV10} to realize positive values. M_8 as a result drains current away from M_7 decreasing V_{DS7} and V_{DS8}; and switching M_9 off. At the switching point, the drain currents of M_9 and M_7 are respectively

$$I_X = \frac{\beta_A(V_X - V_{THN})^2}{2} \tag{8}$$

and

$$I_Y = \frac{\beta_B(V_X - V_{THN})^2}{2} \tag{9}$$

The current in M_9 mirrors that in M_7 at this instant, I_X can therefore be seen as directly proportional to I_Y related by a constant of $\frac{\beta_A}{\beta_B}$. Switching therefore occurs when the βs are equal and the two currents attain equal values. The comparator, however exhibits hysteresis when $\beta_A \neq \beta_B$. Switching point voltages in this case are related to the input transistor transconductance, g_m and differential pair tail current, I_{SS} by:

$$V_{SPH} = -V_{SPL} = v_p - v_m = \frac{I_{SS}}{g_m}.\frac{\frac{\beta_B}{\beta_A} - 1}{\frac{\beta_B}{\beta_A} + 1}, \ for\ \beta_B \geq \beta_A \tag{10}$$

The preamplification stage is loaded with the low impedance diode connected M_7-M_9 transistor pair whiles the cross connected gate M_8-M_{10} pair serve as latch-forming logic inverters which constitute the decision element. The inverter pair transistors are sized such as to achieve a voltage gain larger than unity bearing in mind that they are also loaded by M_7 and M_{10}. Positive feedback from the cross-gate connection was used to increase the gain of the decision element and improve the output state transitions significantly. Typically, comparators tend to produce multiple output transitions when processing slowly-varying signals with even the slightest amount of superimposed noise. This back-and-forth bouncing occurs as a result of the amplification of noise as these signals transition the threshold region. To remedy this issue, some level of hysteresis is introduced into the decision element by choosing different β's in the design. The fractional feedback of the output voltage adds a polarity sensitive offset to the input thereby increasing the threshold range. The output buffer forms the third and final stage of the comparator. This post-amplifier stage converts the output of the second stage into one of two states: V_{DD} or V_{SS}, thereby producing a logic signal. It is a desired characteristic of the output buffer that it is able to accept a differential input signal and exhibit little or no slew-rate limitations. In this design, a self-biased single-ended differential amplifier was employed as the post-amplifier. An inverter was connected to the output of the differential amplifier to provide an additional gain stage and also help isolate any load capacitance from the self-biasing differential amplifier. The diode connected transistor, M_{15} acts as a level shifter to move the decision circuit's output swing into the common-mode range of the differential amplifier.

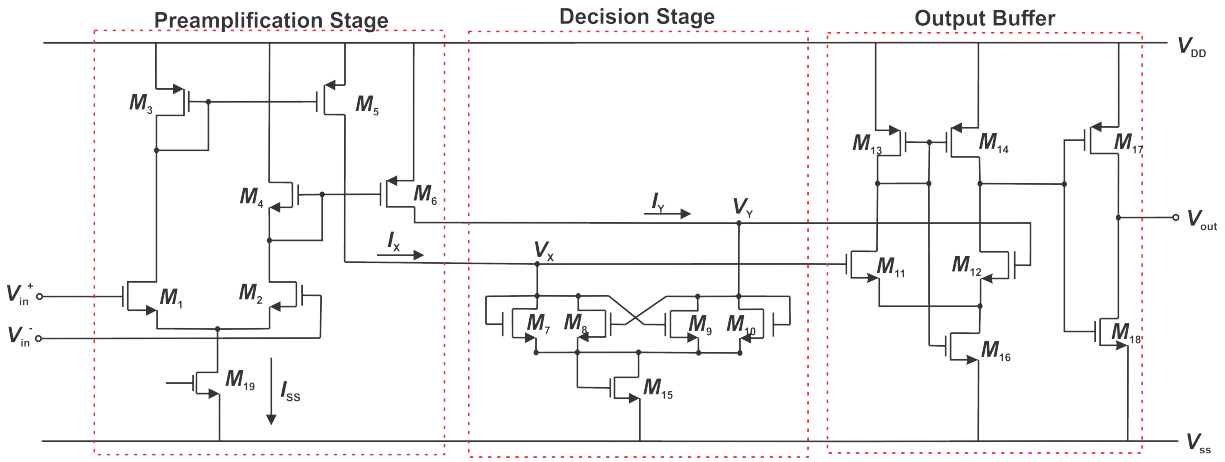


Fig. 2: Proposed comparator design

3.2 Resistor ladder design

The expected power consumption of the resistive ladder was estimated at 78.4μW in a worst case scenario. By having 8 resistors in the string, the value, R, of each resistor was determined from as:

$$R = \frac{V_{REF(MIN)}}{78.4\mu \times 8} \tag{11}$$

where $V_{REF(MIN)}$ is the minimum allowable reference voltage obtained from the comparator design. Voltage quantization involves the approximation of the input signal given a set of fixed reference signals. Unlike Nyquist sampling, which is immune to errors, approximations in quantization introduce noise that cannot be removed [10]. For converters with very low resolution there is a strong relationship between the quantization error and the input signal [9]. Designed as mid-tread type quantizer, the 'staircase' transfer characteristic is shifted by $0.5LSB$ so that code transitions occur around LSB values and the quantization error centred about $0LSB$. To achieve this, the values of the R_{MSB} and R_{LSB} were adjusted from to $1.5R$ and $0.5R$ respectively.

3.3 Encoder design and bubble error correction

The binary encoder designed to convert the 7-bit comparator output to the 3-bit digital word, included a bubble-suppressing logic to remove imperfections from the thermometer code. The bubble-error removal circuitry, which is inserted between the output of the comparators and the input of encoder, has seven 3-input NAND logic gates connected as shown in Figure 3. With this introduction, the logic of encoding is modified such that only the presence of two consecutive '1' logic states right before '0' is indicative of a transition of thermometer code states. The logic table in Table 2 represents the original and revised comparator binary outputs in relation to the expected encoder output word. The Boolean expression that relates the expected output bits to the bubble-suppressing logic output bits are:

$$S_2 = \overline{B_4 B_5 B_6 B_7} = \overline{B_4 B_5} + \overline{B_6 B_7} \tag{12}$$

$$S_1 = \overline{B_2 B_3 B_6 B_7} = \overline{B_2 B_3} + \overline{B_6 B_7} \tag{13}$$

$$S_0 = \overline{B_1 B_3 B_5 B_7} = \overline{B_1 B_3} + \overline{B_5 B_7} \tag{14}$$

The implementation of the encoder is shown in Figure 3

Table 2. : Truth table of the 3-bit binary encoder and bubble removal logic

Comparator Array Output $C_7C_6C_5C_4C_3C_2C_1$	Bubble-Removal Circuit Output $B_7B_6B_5B_4B_3B_2B_1$	Expected Encoder Output $S_2S_1S_0$
0000000	1111111	000
0000001	1111110	001
0000011	1111101	010
0000111	1111011	011
0001111	1110111	100
0011111	1101111	101
0111111	1011111	110
1111111	0111111	111

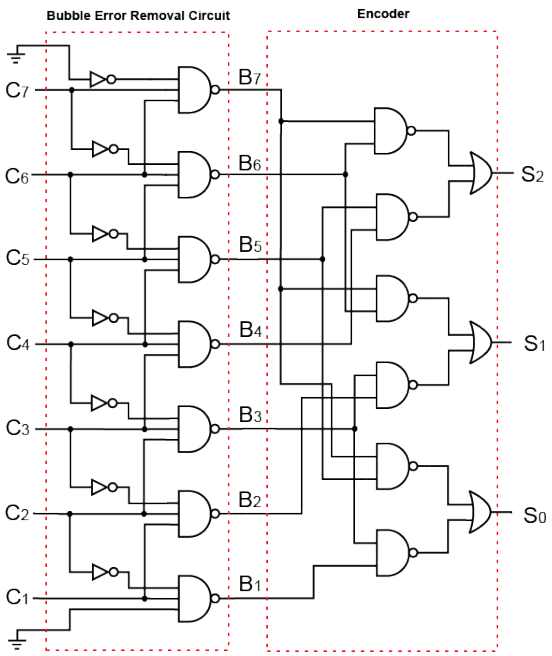


Fig. 3: 3-bit encoder with bubble removal circuit

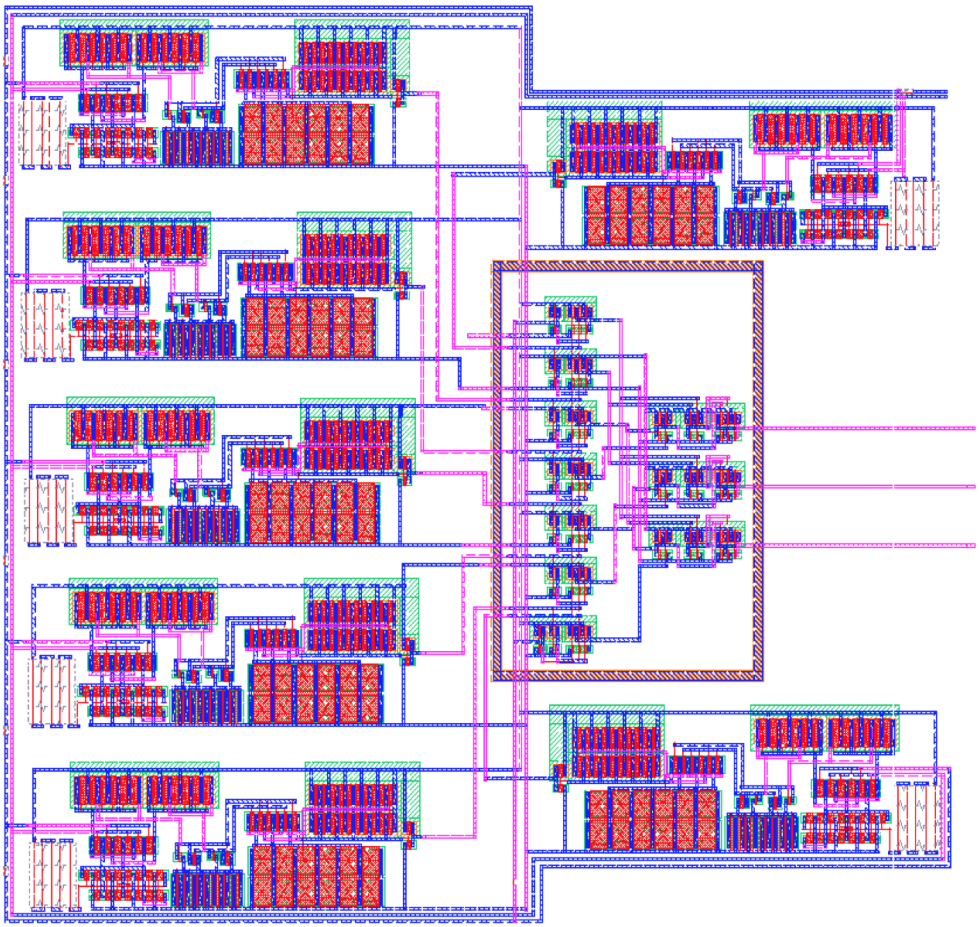


Fig. 4: Layout of the flash ADC in AMI 0.6 μm technology

3.4 Layout

The flash converter layout was realized in the AMI 0.6μm technology is shown in Figure 4. The layout has an area of 343×312 μm^2. Guard rings were placed around the digital circuit to shield the analog circuitry from substrate and power supply noise.

4. SIMULATION RESULTS

The extracted layout of the flash ADC was simulated using the Cadence Spector engine using a rail-to-rail voltage supply of 3V. The power dissipated in each comparator was 3.4mW making the comparator array of 7 comparators dissipate a total power of approximately 23.79mW. The open-loop response of the converter shown in Figure 5 shows a DC gain is approximately 60dB and an operating frequency of 2.17MHz. Transient simulation of the comparator showed that the minimum differential input voltage detectable by the comparator is 34.13 mV. The post-layout comparator simulation metric results are summarized in Table 3.

Table 3. : Post-layout simulation results for each comparator

Parameter	Value
Resolution	34.13 mV
Slew Rate	88.43 V/nS
Propagation Delay	3.21 ns
Sampling Rate	10 MSps

The output of the comparators are shown in Figure 6. The input signal is a ramp voltage signal with the comparator showing the desired output thermometer code. The minimum switching voltage occurred when $V_{IN} = 17.25$mV and the last occurred at $V_{IN} = 227.5$mV. Table 4 shows the various transition voltages for each comparator.

Table 4. : Switches voltages for comparator stack

$V_{IN}(mV)$	$C_7C_6C_5C_4C_3C_2C_1$	$S_2S_1S_0$
$0 \leq V_{IN} < 17.25$	0000000	000
$17.25 \leq V_{IN} < 52.5$	0000001	001
$52.5 \leq V_{IN} < 87.5$	0000011	010
$87.5 \leq V_{IN} < 122.5$	0000111	011
$122.5 \leq V_{IN} < 157.5$	0001111	100
$157.5 \leq V_{IN} < 192.5$	0011111	101
$192.5 \leq V_{IN} < 227.5$	0111111	110
$227.5 \leq V_IN$	1111111	111

The output of the ADC in response to the ramp and a sinusoidal waveform are shown in Figure 7.
Table 5 summarizes a comparison of the post-layout performance simulation results of the designed Flash ADC to some existing works.

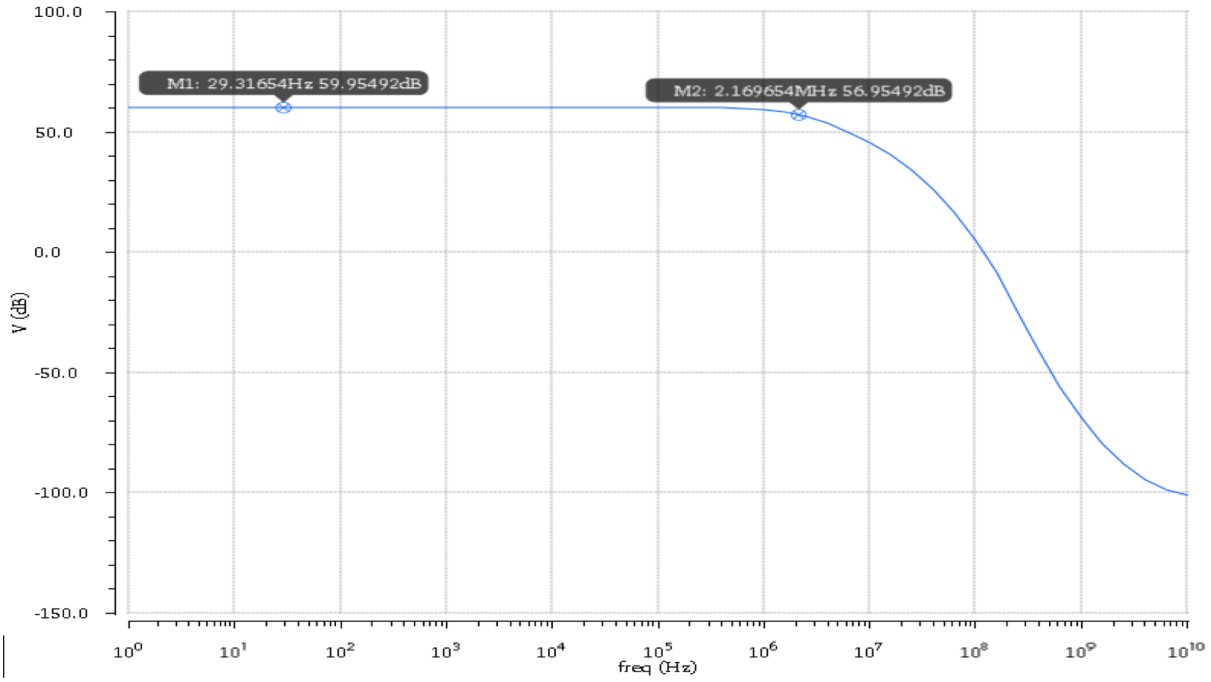


Fig. 5: Frequency response of ADC showing a dc gain of 60dB and a cutoff frequency of over 2MHz.

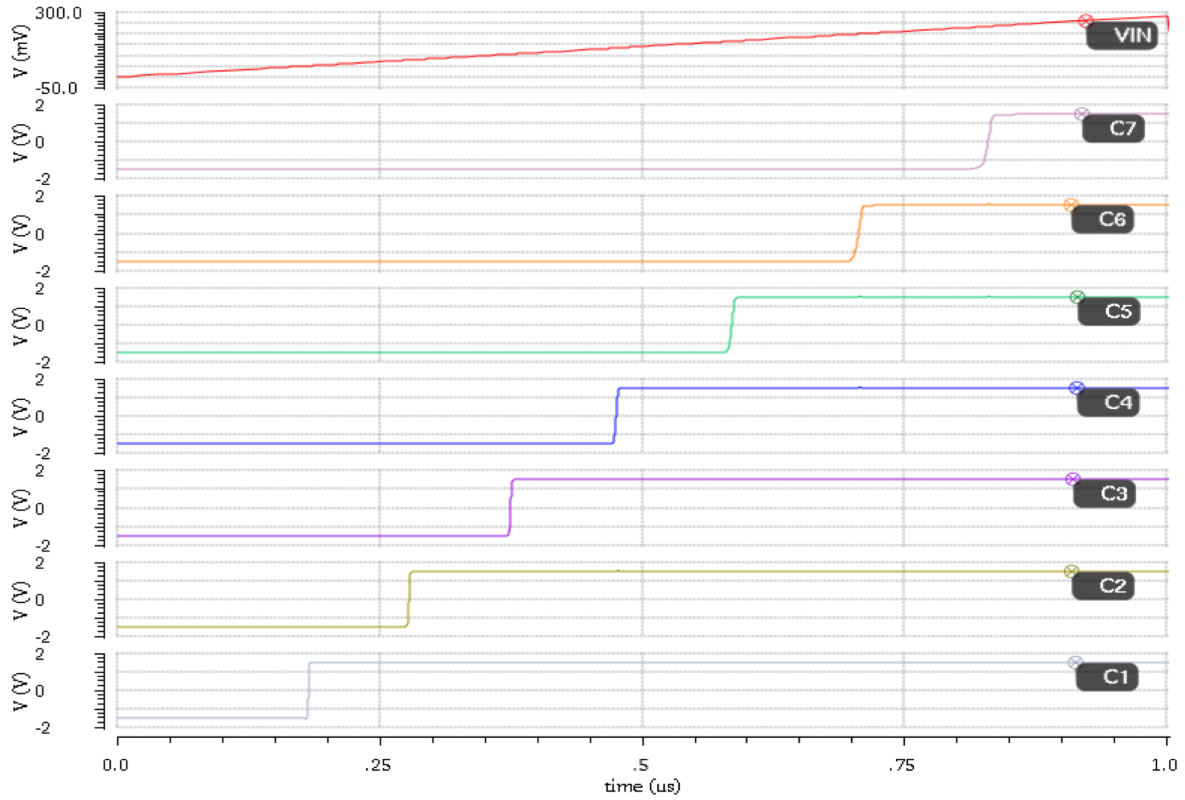
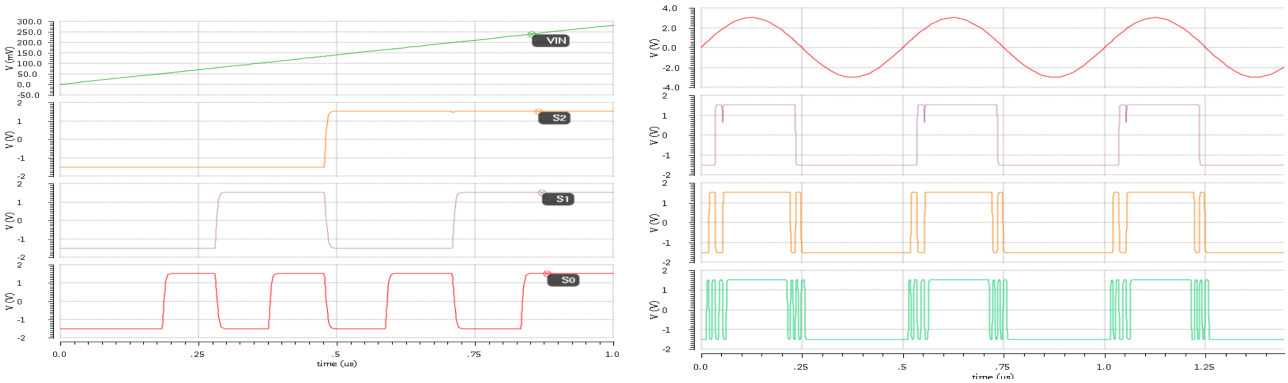


Fig. 6: Output of Comparator with a ramp input voltage



(a) ramp input signal

(b) sine input signal

Fig. 7: Output of the ADC with different input signal waveforms

Table 5. : Comparison of results

Parameter	[3]	[4]	[11]	This work
Technology	180 nm	45 nm	180 nm	600 nm
Resolution	3-bit	3-bit	3-bit	3-bit
Supply voltage	1.8 V	0.7 V	1.3 V	3 V
Speed	-	-	-	10MSps
Power consumption	19.47 μW	218 μW	36.237 mW	23.88 mW
Bandwidth	10MHz	5 MHz	20 MHz	2.17 MHz

5. CONCLUSION

In this paper, a low power 3-bit flash ADC is designed and its performance simulated. The above work outlines the design of the converter in the Cadence®Virtuoso®Analog Design Environment and the device simulation using Spectre®circuit simulator in the AMI06 CMOS technology. The design featured a resistive ladder, three-stage comparators, a bubble noise suppression circuit and an encoder. Simulation results for the design showed a low device power dissipation of 23.7 mW, an input frequency of 2.17 MHz and a conversion speed of 10 MSps achieved with a 3V supply. Results also showed that the transition voltages were a bit different from what was calculated. This was due to the time delay of the comparators and the digital circuit in propagating the signal. The non-ideality introduced into the ADC by adding hysteresis could also be a factor. The designed converter can be used for low power and high speed applications.

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