

Simulation of LTE -Advanced Downlink Physical Layer Transceiver

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ABSTRACT

Due to the growing demands of mobile communication system users, higher peak data bit rates of up to 1 Gbps are being sought. As a result, the Long-Term Evolution Advanced (LTE-Advanced) as an advanced standard for mobile communication systems was created by the Third Generation Partnership Project (3GPP). On the physical layer (PHY), the most recent LTE-Advanced characteristics have been released. In addition to turbo coding, the Downlink uses Orthogonal Frequency Division Multiple Access (OFDMA), whereas the Uplink uses Single Carrier Frequency Division Multiple Access (SC-FDMA). This study uses MATLAB to simulate the LTE-Advanced PHY downlink transceiver in accordance with 3GPP Release 10. The Intra-band contiguous Carrier Aggregation type with two Component Carriers was used to replicate all steps of the LTE-Advanced downlink PHY transceiver, including Time and Frequency Synchronization in the receiver.

Keywords

3GPP release 10; 4G; OFDM; LTE-advanced downlink physical layer; MATLAB

1. INTRODUCTION

The 3GPP has released the complete LTE-Advanced specifications in order to meet the growing demand from customers for faster data speeds in mobile communication systems. Uplink speeds of up to 50 Mbps and downlink speeds of up to 100 Mbps are possible with LTE Release 8. Starting with Release 10, LTE-Advanced was able to achieve peak downlink data speeds of up to 1 Gbps, higher throughput, more coverage, and shorter latencies. [1-14].

The scalable bandwidth of LTE-Advanced is 1.4, 3, 5, 10, 15, or 20 MHz. The LTE-Advanced PHY is a highly efficient data and control transfer facility between the enhanced base station (eNodeB) and the mobile User Equipment (UE). The downlink PHY of LTE-Advanced is OFDMA, while the uplink PHY is SC-FDMA. [15-28].

Carrier Aggregation (CA) should be supported by LTE-Advanced for better data speeds. As a result, CA is viewed as a bandwidth extension option for wide transmission bandwidths ranging from 40 MHz to 100 MHz, as well as a high peak data rate of 500 Mbps in the uplink and 1Gbps in the downlink. Intra-band contiguous uses a single frequency band and is the most straightforward version of CA to implement. [29-36].

The simulation of the LTE-Advanced downlink PHY transceiver with the Intra-band contiguous CA type, as well as time and frequency synchronization in the receiver, is

presented in this work. The simulation platform is MATLAB (version R2014a). The 3GPP version 10 specifications were used to construct the system. Each block in the transmitter and receiver is simulated and verified.

The following sections are arranged in the following order: The design and simulation of the LTE-Advanced transmitter and receiver building blocks, as well as the verification of each block and the overall system, are presented in section two. The CA simulation results are presented in part three, and the conclusion is presented in section four.

2. LTE-ADVANCED TRANSMITTER AND RECEIVER SIMULATION

The LTE-Advanced simulation is created using the 3GPP release 10 specifications and a Frequency Division Duplex (FDD) frame structure. The following are the specifications for the simulated system: The bandwidth is 3 MHz, the number of sub-channels is 15, the number of sub-carriers is 180, the size of the Inverse Fast Fourier Transform (IFFT) and the Fast Fourier Transform (FFT) is 256, the Turbo Encoder/Decoder rate is 1/3, and the system input data is one 96-bit OFDM symbol. [37]. Figures 1 and 2 show the block diagrams of the simulated transmitter and receiver, respectively. All of the building blocks in the transmitter are simulated using MATLAB in the next subsections, and their reverse actions are performed in the receiver. Finally, the complete system (transmitter and receiver) was tested for functionality.

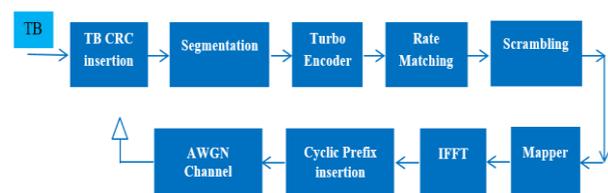


Fig 1: LTE-Advanced downlink physical layer transmitter block diagram [37]

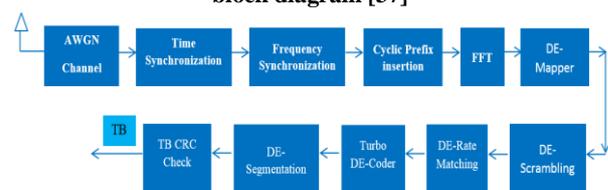


Fig 2: LTE-Advanced downlink physical layer receiver block diagram [37]

2.1 Simulations of CRC and DE-CRC

The Cyclic Redundancy Check is the first block in the transmitter (CRC). This block's purpose is to add 24 redundancy bits to the end of each transport block in order to detect mistakes throughout the block. The polynomial equations of the CRC block were included in the 3GPP Release 10 specifications. The simulation results for the CRC block will be shown in this section. This block's polynomial is known as "gCRC24A" and has the following form [38]:

$$gCRC24A(D) = [D^{24} + D^{23} + D^{18} + D^{17} + D^{14} + D^{11} + D^{10} + D^7 + D^6 + D^5 + D^4 + D^3 + D + 1].$$

where D_n denotes the location that "1" will occupy.

Figure 3 displays the MATLAB simulation command window with the CRC polynomial "gCRC24A" equal to (1 1 0 0 0 0 1 1 0 0 1 0 0 1 1 0 0 1 1 1 1 0 1 1). The number of input bits is requested when the simulation model is run. For example, if 25 ones were entered, Figure 4 depicts the CRC block simulation. This diagram depicts 49 data transmissions (25 ones as input bits plus 24 CRC generated code). Figure 5 depicts the simulation results of the CRC block's final output (transmission data). The DE-CRC procedure is the reversal of the CRC process.

```

gCRC24A = [1 1 0 0 0 0 1 1 0 0 1 0 0 1 1 0 0 1 1 1 1 0 1 1];
input = ones(1, 25);
[rem, crc] = crcmat(input, gCRC24A);

```

Fig 3: The MATLAB code of CRC

crc_field																							
Columns 1 through 17																							
0	1	1	1	1	1	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0
Columns 18 through 24																							
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
data_transmitted																							
Column 1 through 17																							
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Columns 18 through 34																							
1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	
Columns 35 through 49																							
0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Fig 4: The input bits and CRC code from command window

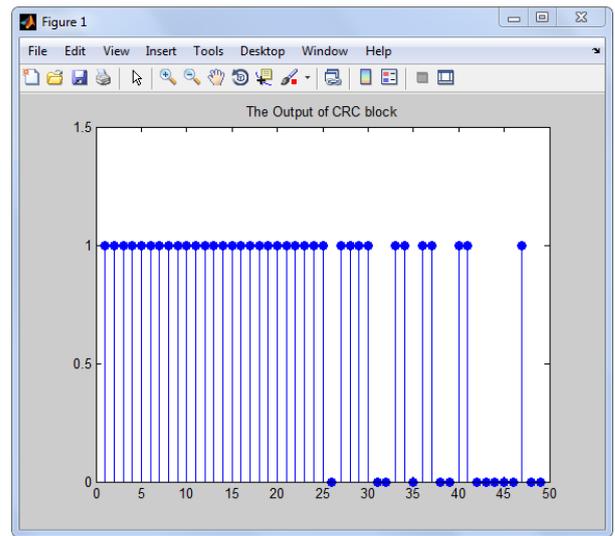


Fig. 5. The final output of the simulation results of the CRC block

2.2 SEGMENTATION and DE-SEGMENTATION

The segmentation block is the second block in the transmitter, and its job is to organize the length of input data so that it may be implemented in the following block, as well as to add a distinct CRC code to each segment to reveal any flaws. Although the Turbo Encoder block can work with transport data input, it only does so in one case: when the length is smaller than 6144. As a result, the input transport block is divided into many segments by the segmentation block. Release 10 section (5.1.2) and table (5.1.3-3) are used to determine the number and length of each segment. [38]. The generating polynomial "gCRC24B," which is stated as follows, is used to determine the CRC code that is inserted at the end of each segment. [38]:

$$gCRC24B(D) = [D^{24} + D^{23} + D^6 + D^5 + D + 1];$$

where D_n denotes the location that "1" will occupy.

In the Matlab workspace, Figures 6 and 7 show the input and output of the segmentation block, respectively. A loopback test is used to verify the segmentation and de-segmentation processes. The segmentation output is applied to the DE-segmentation input in this test. When the segmentation input and the DE-segmentation output are similar, the verification is successful; this is evident when comparing Figures 8 and 9.

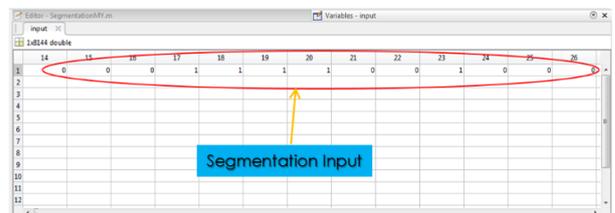


Fig 6: The Segmentation input in Work space

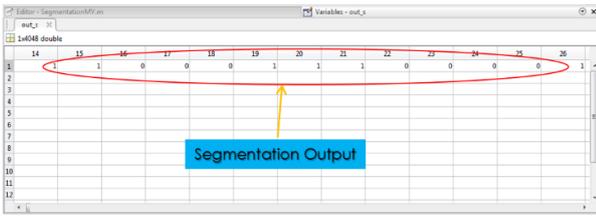


Fig 7. The Segmentation output in Work space

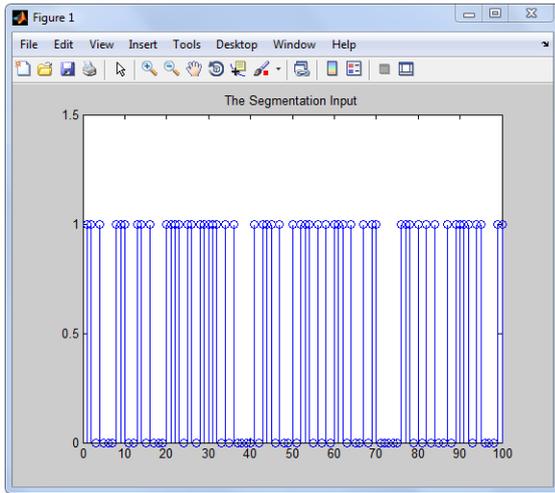


Fig. 8. The Segmentation input

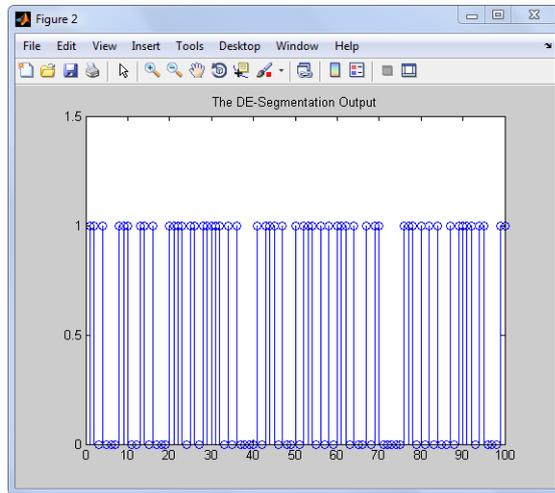


Fig. 9. The output of the DE-Segmentation block in its final simulation

2.3 TURBO ENCODER AND DECODER

As shown in Figure 10, the Turbo Encoder block is mimicked using the Parallel Concatenated Convolutional Code (PCCC) structure. Two 8-state constituent encoders and one turbo code internal interleaver make up this structure; the turbo encoder's coding rate is 1/3. The m-code is used to imitate the Turbo Encoder block. The shift registers of the 8-state encoder were initially populated with zeros. C_0, C_1, \dots, C_{K-1} are the input bits to the turbo code internal interleaver, where K is the number of input bits. The output bits are denoted by the characters, $C'_0, C'_1, \dots, C'_{K-1}, \dots$. The relationship between the turbo code internal interleaver input and the output bits is

defined by the following equation [38]:

$$C'_i = C_{\Pi(i)}, \quad i = 0, 1, \dots, (K - 1)$$

Where the following quadratic form determines the relationship between the output index i and the input index $\Pi(i)$

$$\Pi(i) = (f_1 + f_2) \bmod K$$

The block size K influences the parameters f_1 and f_2 . Table (5.1.3-3) summarizes the parameters f_1, f_2 , and K [38].

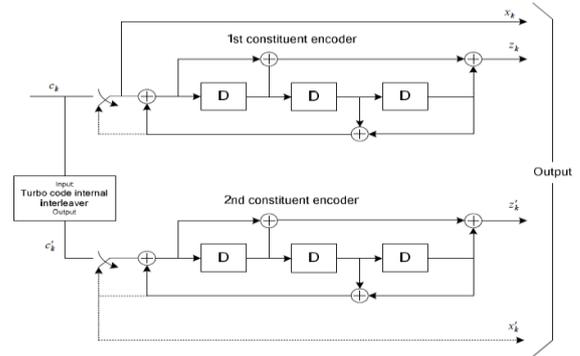


Fig 10: Structure of rate 1/3 turbo encoder [38]

The output of the segmentation block with a length of 100 bits is sent into the Turbo Encoder. The systematic sequence and two parity bit sequences are the Encoder's three outputs. Each of the three outputs has a length of 100 bits. In the command window, Figure 11 shows the testing results of the Turbo Encoder block's input and output. Figures 12 a, b, and c depict the three parallel output sequences (systematic, parity 1, and parity 2), which are determined using the equations below [38]:

$$d_K^{(0)} = x_K, \quad d_{K+1}^{(0)} = z_{K+1}, \quad d_{K+2}^{(0)} = x'_K, \quad d_{K+3}^{(0)} = z'_{K+1}$$

$$d_K^{(1)} = z_K, \quad d_{K+1}^{(1)} = x_{K+2}, \quad d_{K+2}^{(1)} = z'_K, \quad d_{K+3}^{(1)} = x'_{K+2}$$

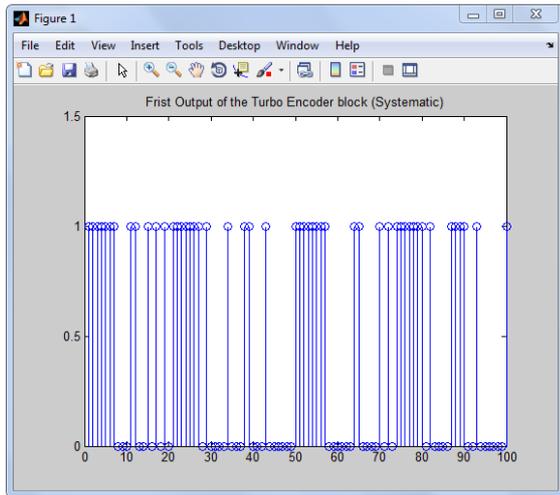
$$d_K^{(2)} = x_{K+1}, \quad d_{K+1}^{(2)} = z_{K+2}, \quad d_{K+2}^{(2)} = x'_{K+1}, \quad d_{K+3}^{(2)} = z'_{K+2}$$

Where K is the number of bits in the input.

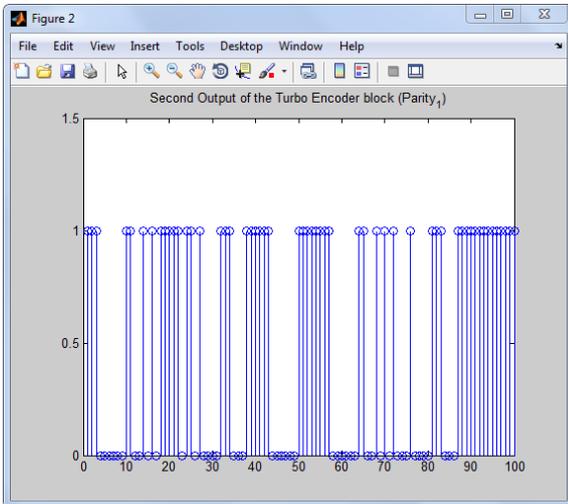
```

Input of MATLAB encoder for 40 bits
[1 0 0 1 0 1 0 1 0 1 1 1 0 1 1 1 0 1 0 1 1 1 0 1 0 1 0 1 1 1 0 1 1 1 0 1]
the output of encoder is
d0 =
Columns 1 through 27
1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1
Columns 28 through 44
1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1
d1 =
Columns 1 through 27
1 1 1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1
Columns 28 through 44
-1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1
d2 =
Columns 1 through 27
-1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1
Columns 28 through 44
-1 1 1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1
    
```

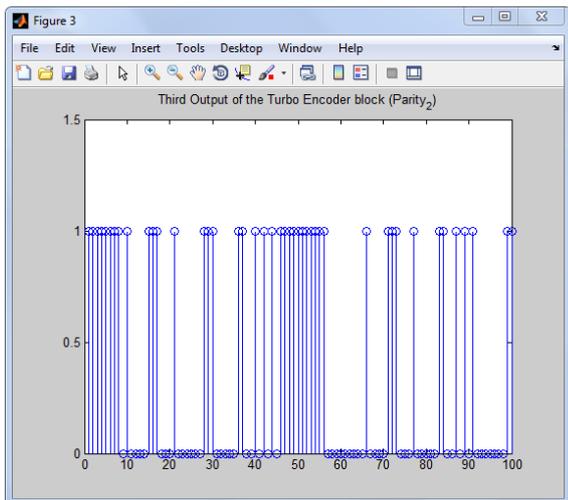
Fig 11: The input and the output testing results of the Turbo Encoder block in command window



a. Systematic (100 bits)



b. The first parity (100 bits)



c. The second parity (100 bits).

Fig 12: The three parallel output sequences of Turbo Encoder

2.4 RATE MATCHING AND DE-RATE MATCHING

The Turbo Encoder block's three parallel outputs are applied to the Rate Matching input, which serves to strengthen data security and immunity to channel defects. The Rate Matching block is made up of three sub-blocks: interleaver, bit collection, and selection; Figure 13 depicts how these sub-blocks interleave.

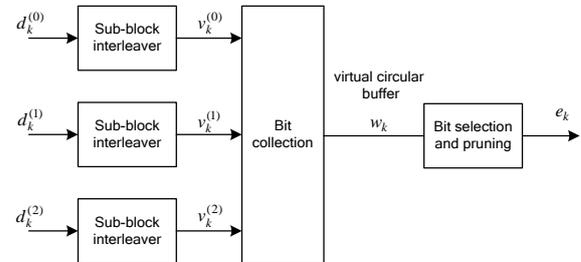


Fig 13: Matching rate block for channels of turbo coding [38]

The Sub-block interleaver's job, according to Release 10 standards, is to arrange the places of the incoming bit stream, as shown in Table 1.

Table 1. Pattern of inter-column permutation for interleaver sub-block [38].

Number of columns $C_{subblock}^{TC}$	Inter-column permutation pattern $\langle P(0), P(1), \dots, P(C_{subblock}^{TC} - 1) \rangle$
32	$\langle 0, 16, 8, 24, 4, 20, 12, 28, 2, 18, 10, 26, 6, 22, 14, 30, 1, 17, 9, 25, 5, 21, 13, 29, 3, 19, 11, 27, 7, 23, 15, 31 \rangle$

The bit collection and selection block's job is to arrange the three parallel outputs from the sub-block interleaves into a single output sequence according to the specification shown in Figure 14 [38]. It is demonstrated that one bit from each sequence is extracted at each round. After that, a bit from the sequence, a bit from the sequence, and so on. The Rate Matching block's final simulation results are shown in Figure 15. The operation of DE-Rate Matching is the inverse of the action of Rate Matching.

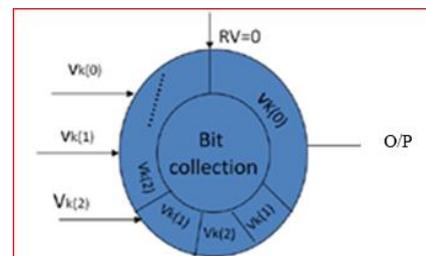


Fig 14: Collection and selection of the transmission bits.

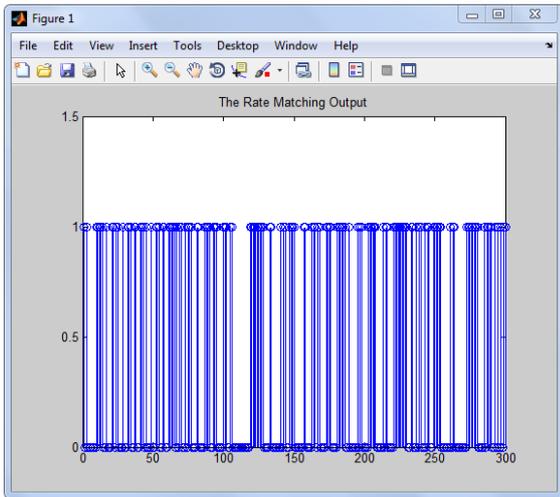


Fig 15. The final result of the matching rate block

2.5 THE SCRAMBLER AND DE-SCRAMBLER

The Scrambler block's job is to increase system security by stopping extended sequences of zeros or ones in transmitted data in order to allow the receiver's clock to regenerate. As shown in Figure 16, the Scrambler block is created using the Pseudo Random Sequence Generator (PRSG) with a length of 31 bits (Gold sequence).

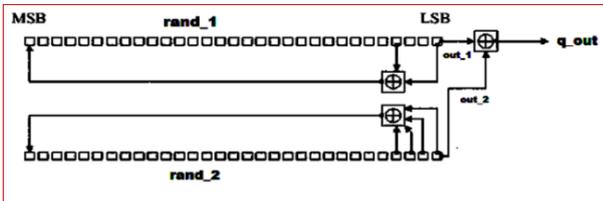
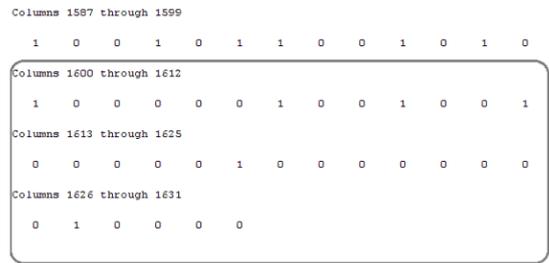
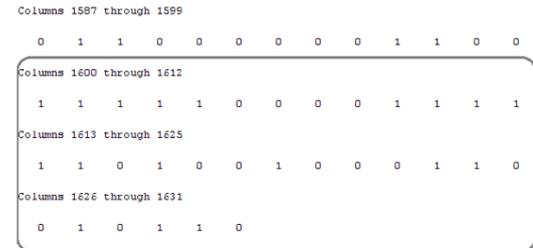


Fig 16: The Generator of Pseudo-Random Sequences (PRSG)

The rand 1 and rand 2 in the PRSG sequence are initialized according to the LTE-Advanced release 10 requirements. The m-code simulates the PRSG sequence. The X-oring operation between the “q out” sequence and the output from the Rate Matching block produces the Scrambler output. The simulation results of the PRSG initialization process from the command window are shown in Figures 17 a and b. The Scrambler code, which is the PRSG's final output, is shown in Figure 18. Figure 19 depicts the X-oring process between the Scrambler input and the Scrambler code, as well as the testing findings of Scrambler output. Figures 20 a and b show the DE-Scrambler block's testing results when the scrambler code is zero or one. The value of the scrambler code determines the DE-Scrambling X-oring operation. When the code value is zero, the output data takes the same shape as the input data. The output is the inverse of the input data when the value is one. The DE-Scrambling data values are the output here. The Scrambler block and the DE-Scrambler operation simulation results are shown in Figure 21.



a: The rand_1 initialization



b. The rand_2 initialization

Fig 17: The initialization of the PRSG sequence.

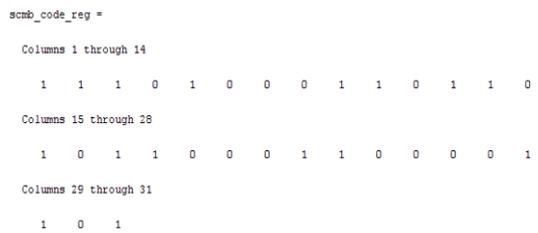


Fig. 18. The Scrambler code



Fig. 19. The Scrambler block's command window testing results



a. The code for scrambler is 0

```

input =
    1 1 0 0 1 0 1 1
    Descrambler Input

scr_code =
    1
    Scrambler code

output =
    0 0 1 1 0 1 0 1
    Descrambler Output
    >>
    
```

b. The scrambler code is one

Fig 20. The DE-Scrambler block test results

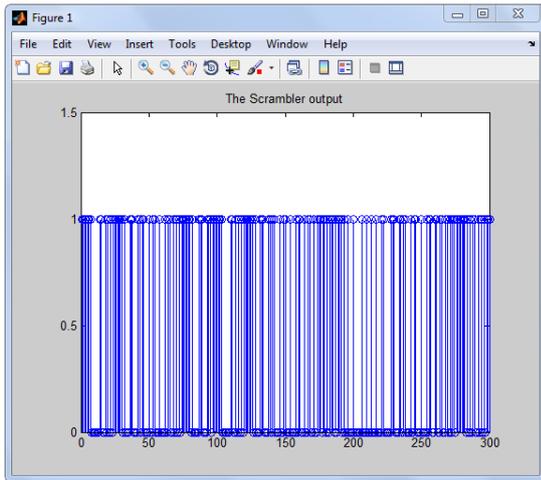


Fig 21. The final Scrambler block output simulation results

2.6 The Mapper and the DE-Mapper

The Mapper with type M-QAM (M=16) is represented by the digital modulation constellation diagram. The output data from the Scrambler block is assigned to the Mapper input by the baseband symbols, which are the I and Q components. The in-phase component is I, and the quadrature component is Q. Figure 22 depicts the 16-QAM Mapper's constellation diagram, Figure 23 depicts the binary scatter plot, and Figure 24 depicts the DE-Mapper block's simulation results.

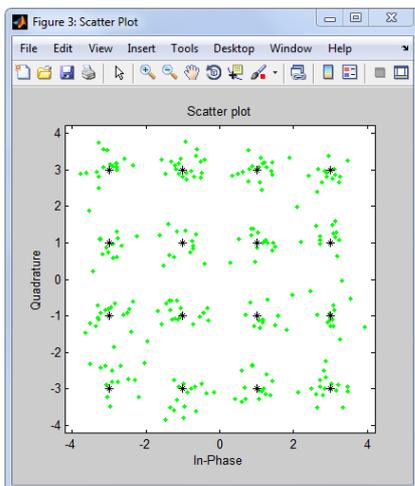


Fig 22: The constellation diagram of the 16-QAM Mapper

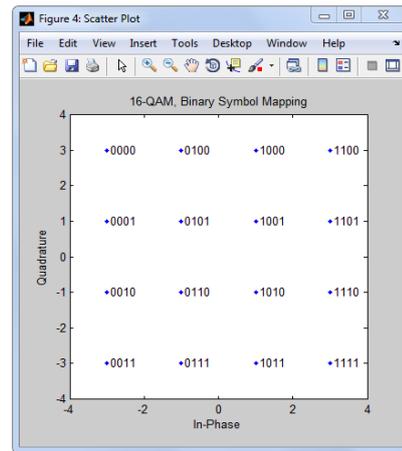


Fig 23: The binary scatter plot of the 16-QAM Mapper

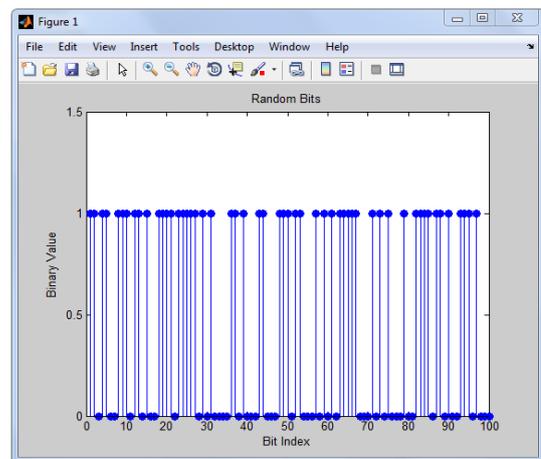


Fig 24. The simulation results of the DE-Mapper block

2.7 The OFDM Signal Generation

The OFDM Signal Generation block in the transmitter comprises an IFFT block and a Cyclic Prefix (CP) insertion block, whereas the receiver does the reverse operations (FFT and Cyclic Prefix removable). The IFFT block's job is to use orthogonal frequency division to improve bandwidth spectral efficiency. The CP insertion block also serves to protect transmitted data from Inter-Symbol Interference (ISI) and Inter-Carrier Interference (ICI). The m-code was used to emulate the IFFT and FFT blocks (with a size of 256) as well as the CP insertion. According to the release 10 standards, CP insertion is accomplished by copying the last 144 samples in the OFDM symbol (for short CP) to the beginning. Figures 25 and 26 depict simulations of the IFFT and FFT blocks' output results, respectively. Figures 27 and 28 depict the insertion of the Cyclic Prefix (the entire OFDM symbol) and removal of the Cyclic Prefix (the last 144 samples in the OFDM symbol) for the short CP, respectively, according to release 10 specifications.

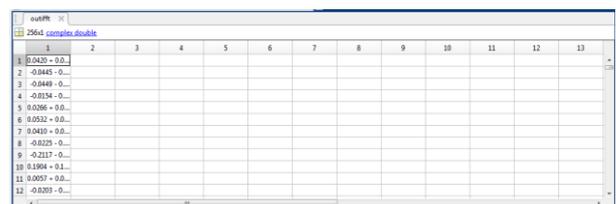


Fig. 25. The IFFT output simulation results.

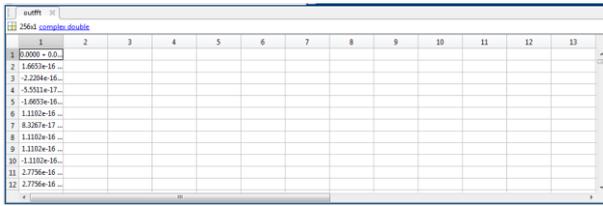


Fig. 26. The FFT output simulation results

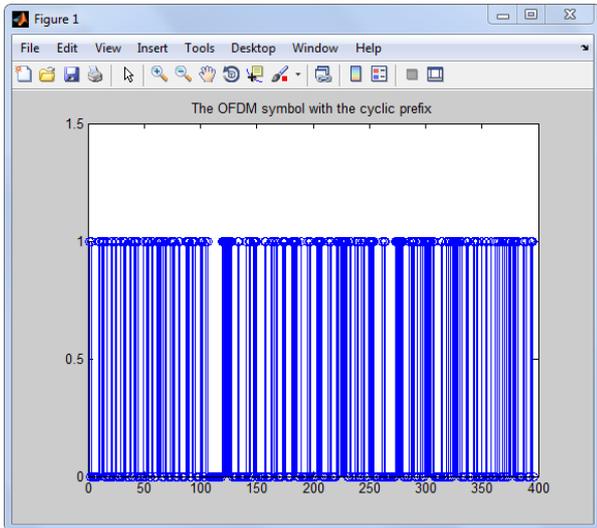


Fig. 27. The OFDM symbol with the cyclic prefix

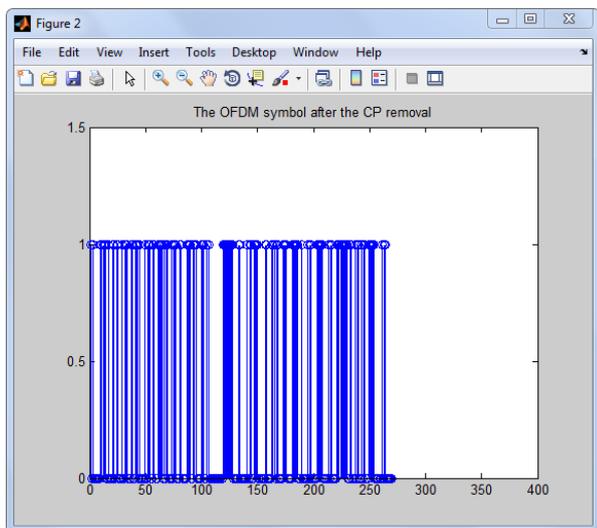


Fig. 28. The OFDM symbol after the CP removal

The loopback test is used to verify OFDM by connecting the output from the OFDM block to the input of the DE-OFDM block. When the input of the OFDM block matches the output of the DE-OFDM block, the verification is complete. Figure 29 depicts the OFDM block's input, whereas Figure 30 depicts the DE-OFDM block's output. The testing findings are clearly the same, indicating that the verification process was completed properly.

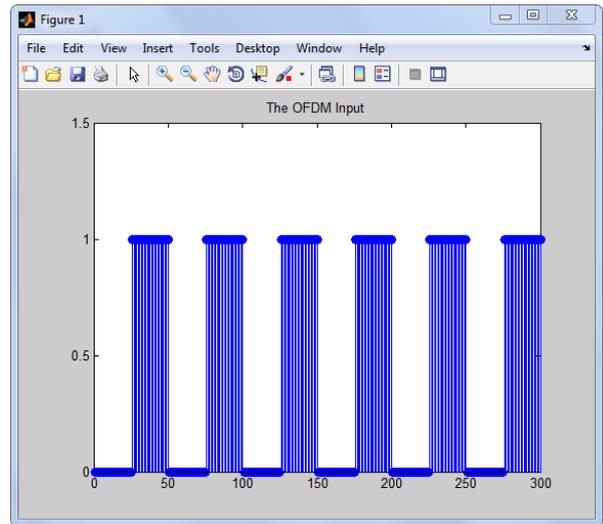


Fig. 29. Input bits to the OFDM block

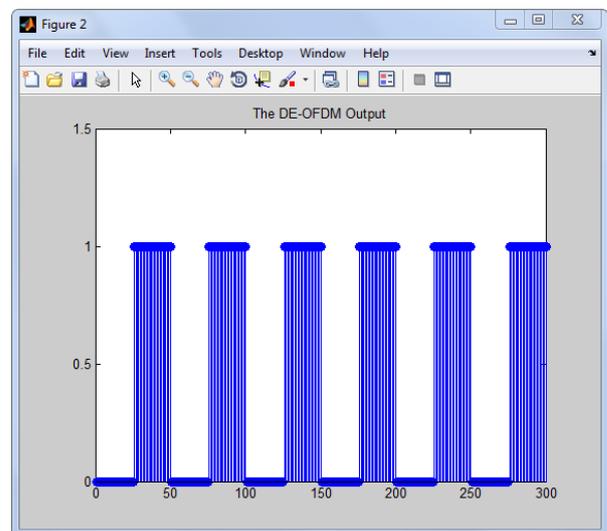


Fig. 30. Output bits of the DE-OFDM block

2.8 Synchronization of Time and Frequency

The Time and Frequency Synchronization blocks are the first two blocks of the receiver. The Time Synchronization block is responsible for determining the start of the OFDM symbol, whereas the Frequency Synchronization block is responsible for determining frequency offsets caused by channel effects such as Doppler shift and carrier frequency mismatching between the transmitter and receiver oscillators. It may be used to determine the Time and Frequency Synchronization values as seen in Figure 31, where the last 144 examples in an OFDM signal are replayed at the beginning.

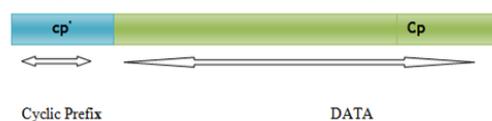


Fig. 31. The symbol for OFDM

The OFDM symbol time T is used to correlate the received symbols with their delayed version during the synchronization phase. The process is then repeated 144 times (CP length) to calculate the sum of the resultant values at each time to obtain the correlation value. After that, the received symbol will shift

one bit and repeats the previous correlation procedure. The correlation results' maximum value is picked and represented in polar form. The OFDM start position and frequency offset values are represented by the amplitude and phase at the maximum correlation value, respectively. The correlation procedure used to generate the Time and Frequency Synchronization values is shown in Figure 32. The following equation is used to calculate the correlation output $X(t)$:

$$x(t) = \int_0^{Tg} r(t-\tau) r^*(t-\tau-T) dt$$

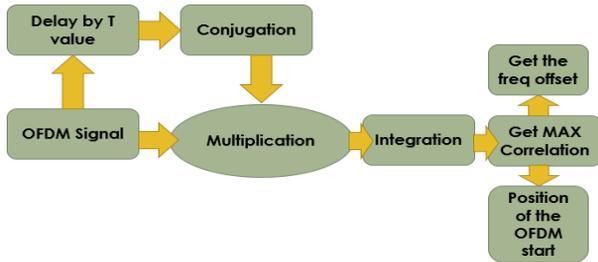


Fig. 32. Cross correlation for frequency and timing synchronization

The 3GPP version 10 specifications do not include the Time and Frequency synchronization theory or equations. The design is constructed and simulated using the theories presented in this section. MATLAB algorithms are used to create and simulate the Time and Frequency Synchronization processes. The sub-sections that follow provide an overview of their simulations.

2.8.1 Simulation of The Time Synchronization

Figure 33 depicts the simulation result of the cyclic extension time synchronization approach. After the cyclic prefix length, the commencement of the OFDM symbol was clearly recognized at sample number 145, as it should be (144 bits).

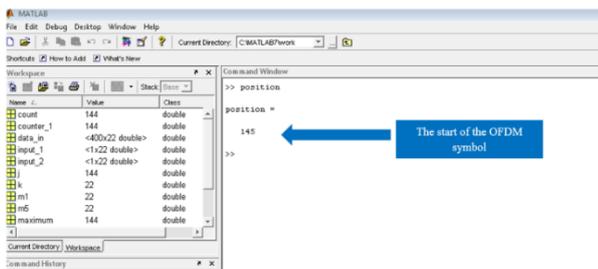


Fig. 33. The results of the time synchronization block

2.8.2. Simulation of the Frequency Synchronization

Figure 34 depicts a simulation of the Frequency Synchronization block. Because the channel impact is only represented by a one-clock-cycle delay, the observed value of the frequency offset is obviously zero.

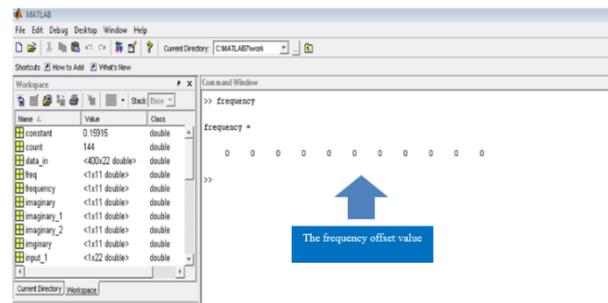


Fig. 34. The results of the frequency synchronization block

2.9 The Full System Simulation

By comparing the transmitter's input to the receiver's output, the complete system is verified. While the transmitter input was represented by one OFDM symbol, the channeling effect was represented by merely a one-clock-cycle delay. The data from the Transmitter's input and the Receiver's output are highlighted in Figure 35. The transmitter's input is obviously the same as the receiver's output. After that, the entire system is successfully verified.

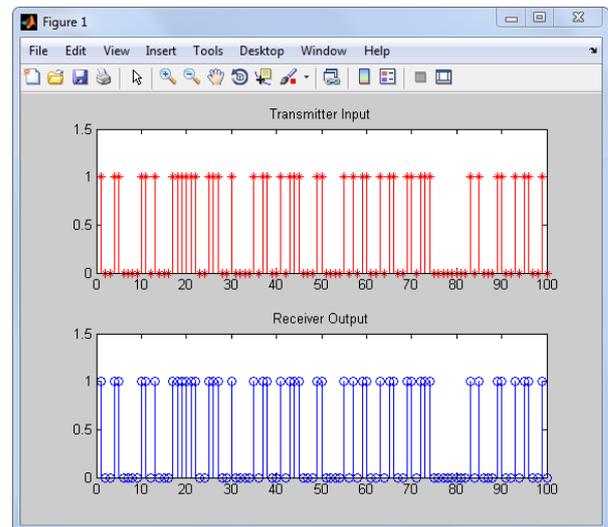


Fig. 35. The Full Simulation of Transmitter input and Receiver output

2.10 The System Noise

This section includes an Adaptive White Gaussian Noise (AWGN) channel effect to examine system noise. By introducing a regulated amount of noise to the transmitted signal, the Bit-error-rate performance might be approximated. The generated signal is fed into the receiver. The receiver then demodulates the signal, resulting in a recovered bit sequence. Finally, using a Bit-Error-Rate vs the energy per bit to noise power spectral density ratio (E_b/N_0) plot, the received bits are compared to the transmitted bits to match up the mistakes. The BER performance of the LTE-Advanced downlink Physical layer via the AWGN channel utilizing the Quadrature Amplitude Modulation (16-QAM) approach is shown in Figure 36. Furthermore, the figure depicts how the BER fluctuates with E_b/N_0 , and it can be seen that the BER lowers as E_b/N_0 increases.

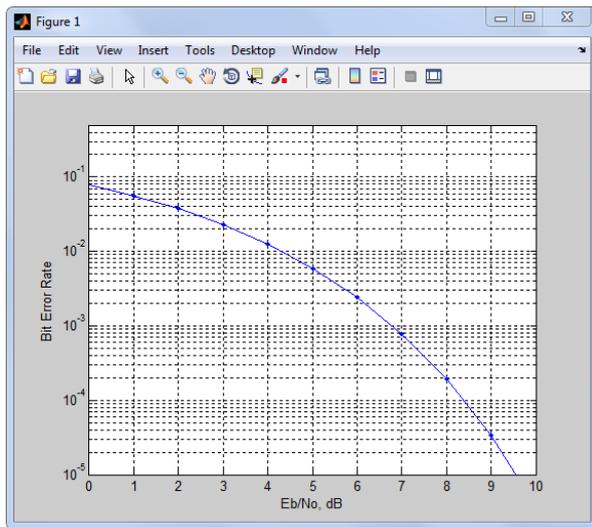


Fig. 36. The system BER performance of AWGN channel

3. CARRIER AGGREGATION SIMULATION

To increase system capacity and data rates, the intra band contiguous carrier aggregation (CA) scenario was implemented. The system data rate is doubled by aggregating two-component carriers (CCs). The Downlink LTE-Advanced simulation is set up to accommodate 6 MHz carrier aggregation using two CCs, each with a bandwidth of 3 MHz. The aggregated carriers' centers have been relocated to the baseband, with the centers of two CCs at -1.5 MHz and 1.5 MHz, respectively. The CA computation is stated in the 3GPP version 10 parts (5.6 and 5.7) in [39]. The definitions of aggregated channel bandwidth, aggregated channel bandwidth edges, and the channel bandwidth for the contiguously aggregated component carriers are highlighted in Figure 37. Figure 38 illustrates the Intra band contiguous CA Power Spectrum with two CC simulation results using the MATLAB application.

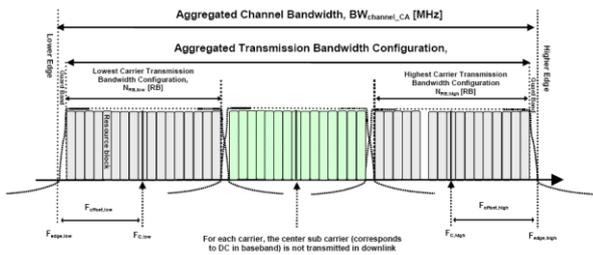


Fig 37: Contiguously aggregated component carriers [39]

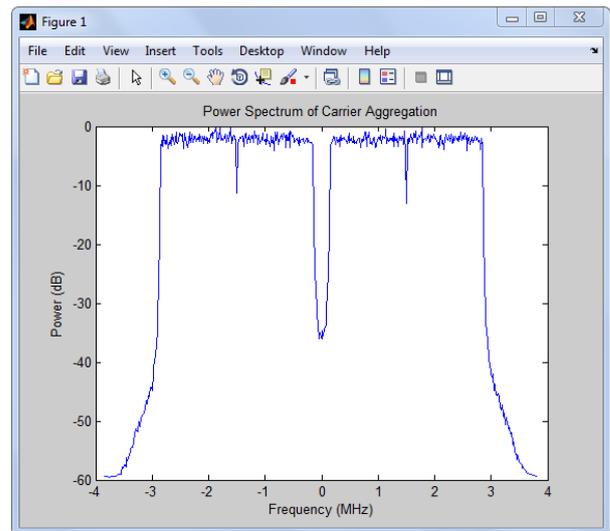


Fig 38: The Power Spectrum of the two Component Carriers

4. CONCLUSION

The building blocks of a complete LTE-Advanced downlink physical layer transceiver with the Intra-band contiguous CA type were constructed and simulated in this study using MATLAB, according to the 3GPP release 10 standards. Aside from the time and frequency synchronization blocks in the receiver, all of the blocks in both the transmitter and receiver were simulated and confirmed. The CA approach was shown to give high data rates and higher system capacity in the LTE-Advanced downlink system. The data rate was doubled after utilizing the Intra-band contiguous CA type with two CC, and the predicted system data rates were enhanced by increasing the number of using CC, according to the simulation results.

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