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Crosstalk Noise Modeling analysis for RC Interconnect in Deep Sub-Micron VLSI Circuit

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ABSTRACT
This thesis presents an approach to solve the VLSI (very large scale integration) layer assignment problems that will lead to the minimization of crosstalk noise. Using 2π model a closed form crosstalk noise modeling for on-chip VLSI RC interconnects is presented in this thesis. The interconnection can be modeled as distributed RC segments with sufficient accuracy for the low frequency of operation. When step input and saturated ramp input is applied to the aggressor which is adjacent to the victim net then this crosstalk noise modeling is perpetrated. In this thesis, the working model represents the noise voltage waveform. This thesis is worked to find out noise pulse width and noise amplitude for RC interconnection. In this thesis, the original 2π model is further simplified and it has simply closed form expressions, which is capable of measuring noise pulse width and noise amplitude for RC interconnect. The closed form expressions of a 2π model are simulated using Matlab. This model considers various parameters, such as coupling location (near the driver and near receiver) and course distributed RC characteristics for victim net.

Keywords
Deep sub-micron, Noise modeling, Crosstalk, RC interconnect, Step input, Ramp input, VLSI.

1. INTRODUCTION
After the invention of integrated circuit (IC) there have been several advances in the technology that led the way the ICs are fabricated. This significant fabrication was possible only by reducing the feature sizes of the CMOS transistor. According to the National Technology Roadmap for Semiconductors (NTRS), feature size will further decrease at the rate of 0.7× per generation. Designing of VLSI circuits have entered into deep sub-micron (DSM) design phase. DSM technology means, using transistors of smaller size with faster switching rates. Technologies beyond the feature sizes of 0.25 μm are usually referred as DSM technologies. Several challenging issues in DSM technology are low power design signal integrity, high density and design complexity, packing and testing, cost-effective approach. Signal integrity is one of the major challenges that the DSM technology faces. The major concerning signal integrity issues are crosstalk delay, crosstalk noise, IR (voltage) drop in power lines, electro-migration and manufacturing-related issues that if not addressed can lead to chip failure. Crosstalk delay and crosstalk noise are the primary effects of the increased coupling capacitance. The coupling capacitance tends to be more significant in modern process technologies due to small and narrow feature sizes. The net under analysis which suffers from coupling noise is referred to as victim, and all neighboring nets which contribute to coupling noise on the victim are termed as aggressors. There are many appropriate measurements to minimize crosstalk noise for RC interconnects in DSM VLSI circuits. Cross talk noise modeling approaches are loosely classified into two categories based on their trade off between accuracy and efficiency. They are analytical modeling and simulation. The popular analytical models are Devgan[1], Heydari[2], Vital[3], Kuhlmann[1.10]. But the drawback of these models is that they deal with fully coupled structures and hence are not suitable for partially coupled lines. In this thesis we used a 2π RC interconnect crosstalk noise model [4] , which can accurately deal with partially coupled lines. Compared with previous crosstalk noise models the 2π model is proven to be more accurate. The main objective of this thesis is to study analytically of the 2π model based cross talk noise model for RC interconnects in deep sub-micron VLSI circuits for both unit step and saturated ramp inputs. Another objective is to simulate the analytical study results in MATLAB (R2007b) environment. This paper is summarized as follows: Section II material and method, Section III shows and describes the simulation results. Finally Section IV concludes the paper.

2. MATERIALS AND METHODS
In this section, At first present the 2π model approach and derive its analytical time domain waveform for both unit step and saturated ramp inputs.Then it's focus on two key metrics for the 2π model, i.e., peak noise amplitude and noise width.Finally it's simulate the noise amplitude and noise width using MATLAB (R2007b) Softwere.

2.1 Derivation Of 2π Model
In this study, victime network is considered as a RC line. An aggressor line is placed near the victim net, as shown in Figure 1. The aggressor voltage pulse at the coupling location be both unit step and saturated ramp inputs. As seen in the Figure 2, L_s represents the interconnect length of victim net before the coupling. Similarly, L_c, L_e represent the interconnect length of victim net at the coupling and after the coupling, respectively. 2π model is reduced to a 2π type RC model as shown in Figure 2. This reduction of 2π model is very useful while calculating the value of crosstalk noise at the receiver end. This model contains two π type RC circuits, known as 2π model. One RC circuit is located before the coupling and the other is after the coupling. The victim driver is modelled by an effective resistance R_d and other RC parameters are C_x, C_1, R_s, C_2, R_e and C_L.

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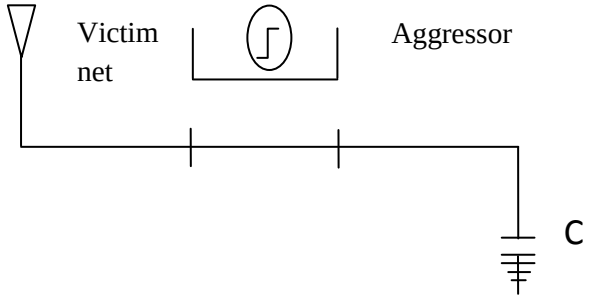

Figure 1 Layout of a victim net and an aggressor above it.

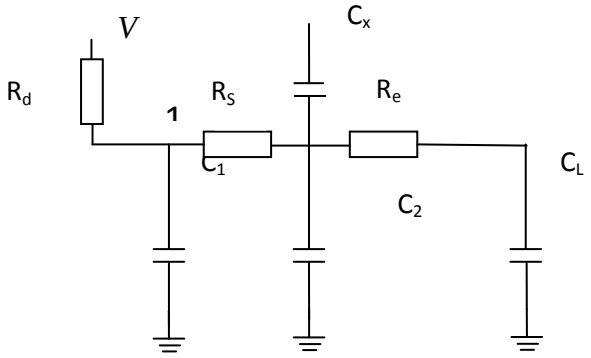

Figure 2 2π Model Crosstalk Noise Model

The coupling node (noad 2) is set to be the center of the coupling portion of the victim net, i.e. $L_s+L_c/2$ from the source. Let the upstream and downstream interconnect resistance/capacitance are $R_s/C_s$and R_e/C_e, respectively. Then capacitance values are set to be $C_1 = C_s/2$, $C_2 = (C_s+C_e)/2$ and $C_L = C_e/2+C_1$. In some cases one lumped RC for the victim net can be used, but 2π model can model the coarse distributed RC characteristics. The resulting 2π model can be solved analytically [4]. According to figure 2 the impedance at node 1, Z_1 satisfying the following.

$$\frac{1}{Z_1} = \frac{1}{R_d} + sC_1$$

Then at noad 2, we have

$$\frac{1}{Z_2} = \frac{1}{(z_1 + R_s)} + sC_2 + \frac{1}{\left(R_e + \frac{1}{sc_l}\right)}$$

The s-domain voltage $V_2(s)$ at point 2, across the impedance Z_2 satisfying the following

$$V_2(s) = \frac{Z_2}{Z_2 + \frac{1}{sC_x}} V_{agg}(s)$$

The output voltage V_{out} in the s-domain is

$$V_{out}(s) = V_2(s) \frac{\frac{1}{sC_l}}{R_e + \frac{1}{sC_l}} \qquad (1)$$

Substituting Z_1, Z_2, and V_2 into V_{out} (s) yields,

$$V_{out}(s) = \frac{a_2 s^2 + a_1 s}{s^3 + b_2 s^2 + b_1 s + b_0} V_{agg}(s) \qquad (2)$$

Where the coefficient are

$$K_1 = R_d R_s C_1 C_x$$

$$K_2 = R_d R_s C_1 C_L R_e (C_x + C_2)$$

$$a_1 = \frac{C_x(R_d + R_s)}{K_2}$$

$$a_2 = \frac{K_1}{K_2}$$

$$b_1 = \frac{(C_x + C_2)(R_d + R_s) + (R_d C_1 + C_L R_e) + C_L(R_d + R_s)}{K_2}$$

$$b_2 = \frac{(C_x + C_2)\{R_d R_s C_1 + C_L R_e\} + \{R_d R_e C_1 C_L + R_d R_s C_1 C_L\}}{K_2}$$

$$b_0 = \frac{1}{K_2}$$

Noise Amplitude and Width Calculation for Unit Step Input

For the aggressor with unit step input with normalized V_{dd} = 1, i.e.

$$V_{agg} = \begin{cases} 1 & t \geq o \\ 0 & otherwise \end{cases}$$

Its Laplace transform is, $V_{agg}(s) = \frac{1}{s}$

Noise Amplitude Calculation

On simplifying equation (2) using dominant-pole approximation method,

$$V_{out}(s) = \frac{a_1 s}{b_1 s + b_0} V_{agg}(s)$$

Where,

$$V_{agg}(s) = \frac{1}{s}$$

So, $V_{out}(s) = \frac{t_x}{t_v\left(s + \frac{1}{t_v}\right)}$ (3)

Here, $C_x(R_d + R_s) = t_x$

And $(C_x + C_2)(R_d + R_s) + (R_d C_1 + C_L R_e) + C_L(R_d + R_s) = t_v$The term t_x represents the RC delay term from the upstream resistance of the coupling element times the coupling capacitance. The term t_v represents distributed Elmore delay of victim net. The output voltage shown in (3) can be expressed in time domain and given in (4).

$$V_{out}(t) = \frac{t_x}{t_v} e^{-t/t_v}, \qquad where\ t \geq 0 \qquad (4)$$

From the noise expression shown in (3.15), it is evident that noise monotonically decreases as $t \geq 0$. The value of noise will be maximum at t = 0. This maximum value of noise can be calculated by putting t = 0 in (4).

$$V_{max} = \frac{t_x}{t_v} \qquad (5)$$

Noise Width Calculation

The noise width for a noise pulse is defined to be the length of time interval so that the noise spike voltage V is larger than or equal to V_t

Where Vt represents the threshold voltage. Now from equation (4),

$$V_{out}(t) = \frac{t_x}{t_v} e^{-t/t_v}$$

$$t = t_v \ln\left(\frac{1}{V_{out}} \frac{t_x}{t_v}\right) \quad (6)$$

Noise width is the width of time interval between t_1 and t_2.

Here t_1= initial time = 0

And t_2 is the time when noise voltage is equal to the threshold voltage V_t

The value of t_2 can be calculated using (6). Hence, $t_2$can be derived as,

$$t_2 = t_v \ln\left(\frac{1}{V_t} \frac{t_x}{t_v}\right)$$

Noise width is given by,

$$t_{width} = t_v \ln\left(\frac{1}{V_t} \frac{t_x}{t_v}\right) \quad (7)$$

In this paper, we assume the value of threshold voltage $V_t$to be half of the value of the peak noise voltage V_{max}.

$$i,e. V_t = \frac{V_{max}}{2} \quad (8)$$

Now from equations (5), (7) and (8)

$$t_{width} = t_v \ln(2) \quad (9)$$

This expression represents the width of the noise voltage waveform. For unit step input, note that when the time increases beyond t_2, the noise voltage becomes very less. In the above calculation we ignored the effect of that noise. In some conditions peak noise exceeds certain threshold voltage but remains immune to the noise. This can be expressed clearly by some noise amplitude versus noise width plots.

Noise Amplitude and Width Calculation for Saturated Ramp Input

The aggressor with saturated ramp input with normalized V_{dd} = 1 and transition time t_r, then,

$$V_{agg} = \begin{cases} t/t_r & 0 \le t \le t_r \\ 1 & t \ge t_r \end{cases}$$

Its Laplace transformation is

$$V_{agg}(s) = \frac{1 - e^{-st_r}}{s^2 t_r} \quad (10)$$

Noise Amplitude Calculation

On simplifying equation (2) using dominant-pole approximation method,

$$V_{out}(s) = \frac{a_1 s}{b_1 s + b_0} V_{agg}(s)$$

$$V_{out}(s) = \frac{t_x(1-e^{-st_r})}{st_r(st_v+1)} \quad (11).$$

Computing the inverse Laplace transform of equation (11), we can obtain the time domain waveform

$$V_{out}(t) = \frac{t_x}{t_r}\left(1 - e^{-t/t_v}\right) \quad (12)$$

Where, $0 \le t \le t_r$

And,

$$V_{out}(t) = \frac{t_x}{t_r}\left(e^{-(t-t_r)/t_v} - e^{-t/t_v}\right) \quad (13)$$

Where, $t \ge t_r$

From the noise expression shown in (12) and (13), it is easy to obvious that noise monotonically increase at $0 \le t \le t_r$ and decreases at $t \ge 0$. So the value of noise will be maximum at $t = t_r$. This maximum value of noise can be calculated by putting $t = t_r$ in both equations (12) and (13) and we get.

$$V_{max} = \frac{t_x}{t_r}\left(1 - e^{-t_r/t_v}\right) \quad (14)$$

Noise Width Calculation

Given certain threshold voltage V_t, the noise width for a noise pulse is defined to be the length of time interval so that the noise spike voltage V is larger than or equal to V_t.

$$V_t = \frac{t_x}{t_r}\left(1 - e^{-t_1/t_v}\right)$$

$$t_1 = t_v \ln\left(\frac{t_x}{t_x - t_r V_t}\right) \quad (15)$$

$$t_2 = t_v \ln\left\{\frac{t_x}{t_r V_t}\left(e^{t_r/t_v} - 1\right)\right\} \quad (16)$$

Noise width is the width of time interval between t_1 and t_2.

$$t_{width} = t_2 - t_1 \quad (17)$$

In this thesis, it is assume the value of threshold voltage V_t to be half of the value of the peak noise voltage V_{max}.

$$i,e. V_t = \frac{V_{max}}{2} \quad (18)$$

Now from equations (15), (16),(17) and (18)

$$t_{width} = t_r + t_v \ln\left[\frac{1 - e^{-2t_r/t_v}}{1 - e^{-t_r/t_v}}\right] \quad (19)$$

3. RESULTS AND DISCUSSIONS

The 2π model estimates the peak noise and noise width for unit step input. The model has been tested extensively and its accuracy has been compared with circuit simulation results. Some circuits with different parameter values have been taken and tasted. We run 2π model, Devgan model [1], Heydari [2], Vittal model [3], and circuit simulations on 1500 randomly generated circuits in 0.18 µm technology. For the test circuits, the driver resistance R_d is from 20 to 200 Ω, the loading capacitance C_L is from 4 to 50 fF and the aggressor slew is forming 10 to 500 ps.

From Figure 3 we can easily see that amplitude of the noise voltage monotonically decrease with respect to time. When time much increases then the amplitude of the noise voltage

become very low. Maximum voltage is 0.266 V, threshold voltage is 0.133 V and noise width is 100 ps.

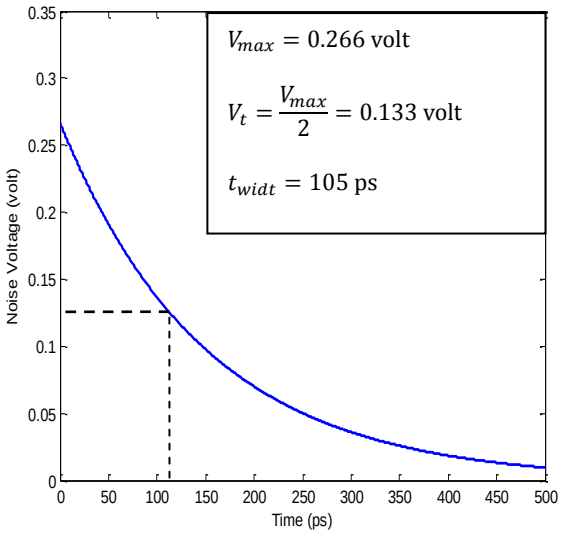

Figure 3 Noise voltage for unit step input when 2π model is used

From Figure 4 it can easily see that amplitude of the noise voltage monotonically increase and decrease with respect to time. Maximum voltage is 0.433 V and threshold voltage is 0.216 V, noise width is 10.5 ps

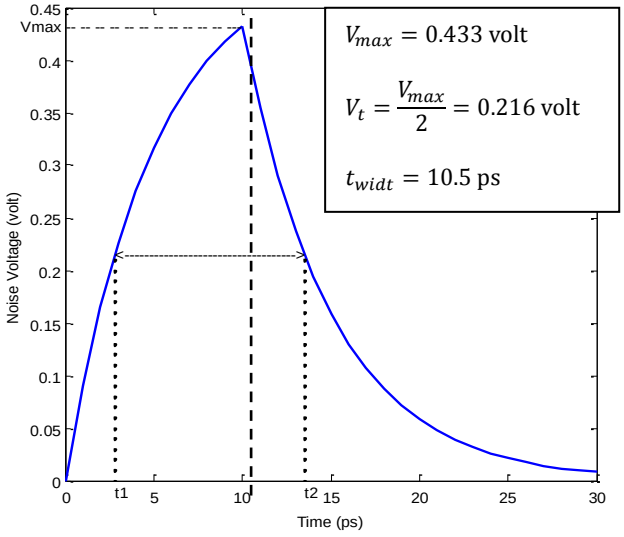

Figure 4.Noise voltage for saturated ramp input when 2π model is used

Figure 5 shows the changes in maximum crosstalk noise voltage when the input rise time varies from 10 ps to 200 ps and all of the geometric parameters are kept constant. As seen in the figure the. 2π model is compared with Devgan named as DEV, Heydari named as HAY and circuit simulation.

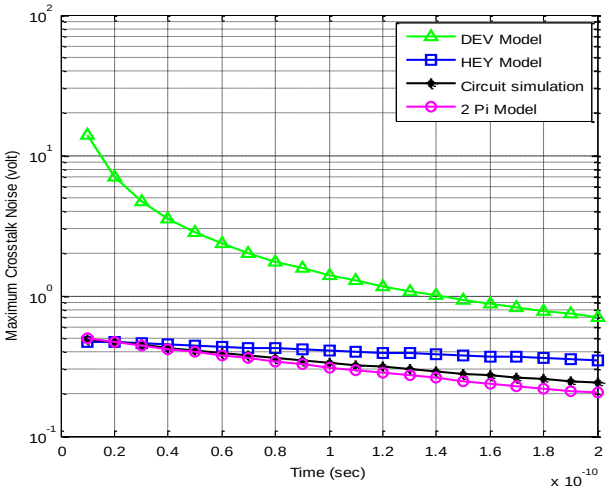

Figure 5 Maximum Crosstalk noise voltage of two coupled RC transmission line for unit step input

Figure 6 shows the scatter diagram comparing the Devgan model, Heydari model and 2π model (Y-axis) with circuit simulations (X-axis) for 15 randomly generated four-pin nets. The investigation setting is the same as those for 2-pin nets. The branching wire length ranges from 1to 2000μm. The branching location can be anywhere from driver to receiver. Circuit simulations are performed on distributed RC networks by dividing each long wire into every 10 μm segment. Compared with circuit simulation, the estimation accuracy of 2π model is higher than others models. Figure 4.8 shows that 2π model versus circuit simulation RC trees for noise width.

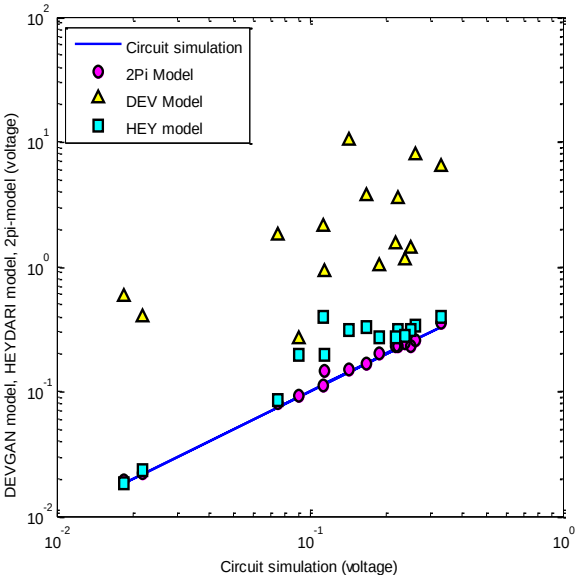

Figure 6 Comparison of pick noise voltages among different models for unit step input.

We have taken 15 values of parameters (such as, resistor, capacitor, coupling capacitor, wire length) which is given in Table 1. All these parameters values put in the noise amplitude expression and analyze the performance of different models. Table 1 demonstrates the accuracy of the 2π model in calculating the peak noise amplitude of the coupling noise of two capacitively coupled interconnects in the presence of the unit step input at the input of the aggressor net. The noise estimation of the 2π model is compared with

circuit simulation. From Table 1 we notice that 2π model has the highest estimation of noise amplitude.

Table 1: Peak noise calculation for different models[2].

SPIE volts	**Devgn volts**	**Heydi volts**	**Vittl volts**	**2π Volts**
0.189	1.0039	0.2731	0.2106	0.201
0.331	6.33353	0.3988	0.401	0.353
0.143	10.2	0.3101	0.2	0.15
0.168	3.6652	0.3287	3.6652	0.166
0.113	2.0832	0.3991	2.0832	0.111
0.26	7.8097	0.3360	7.8097	0.256
0.222	3.4753	0.3062	3.4753	0.231
0.25	1.4040	0.3100	1.4040	0.23
0.219	1.5054	0.2688	1.5054	0.230
0.144	0.9136	0.1969	0.9136	0.145
0.075	1.7857	0.0851	1.7857	0.08
0.238	1.1232	0.2788	1.1232	0.24
0.0218	0.3948	0.0232	0.3948	0.0221
0.0185	0.5772	0.0185	0.5772	0.0192
0.0901	0.2670	0.1975	0.2670	0.0932

The mean and maximum error values are reported in Table 2. These tables testify to the higher accuracy of the 2π approach compared to these other approaches. More precisely, the 2π analytical model results in an average estimation error of only 3.7% which is better than the 28.30% average estimation error resulting from the method[3]. Interestingly, the 2π model exhibits a better accuracy compared to [3] when the driver sizes of aggressor and victim lines are hugely different. Our thesis shows that the average errors for peak noise estimation using Devgan model , Vittal model, Heydarimodel and 2π model are 1558%, 28.30%, 55.83% and less than 4%, respectively. The average errors for peak noise width less than 4%.

Table 2: Percentage error comparison for 2π model and other three models [2]

	Devgan (%Error)	Heydari (%Error)	Vittal (%Error)	2π Model (%Error)
	431	44.4974	11.42	6.3492
	1813	20.4834	21.14	6.6465
	7033	116.8531	39.9	4.8951
	2082	95.6548	25.65	1.1905
	1744	253.1858	23.53	1.76
	2904	29.2308	25	1.5385
	1465	37.9279	22	4.0
	462	24.0000	4	8.0
	587.4	22.7397	21.46	5.0
	534.4	36.7361	31	0.6944
	2280	13.4667	34.66	6.6667
	371.9	17.1429	28.15	0.8403
	1711	6.4220	37.61	1.3761
	302	0	62.16	3.7838
	196	119.2009	36.95	3.4406
Average	1558	55.83	28.30	3.7
Minimum percentage error	196	0	4	0.6944
Maximum percentage error	7033	253.1858	62.16	6.6667

It can be found that using the 2π model both peak noise and noise width calculation results in an error of as less as when compared with those of circuit simulations, and almost 97% nets have less than 6% errors. So, the 2π model is best for crosstalk noise estimation for interconnect in deep sub-micron VLSI circuit. Table 3 notice that the percentage error of noise width for 2π model.

Table 3: Noise width percentage error for 2π model [2]

t_{width} (%Error)	Average	Minimum	Maximum
2.2913 0.0776 6.1694 2.6769 3.80 6.10 6.25 2.7273 2.9412 5.2632 2.8571 3.2258 3.30 3.57 2.6786	3.595	0.0776	6.25

4. CONCLUSION

It's focused on the analysis and modeling of crosstalk noise for RC interconnects in deep sub-micron VLSI circuits. We study several approaches as, Devgan model, Heydari model,

Vittal model and 2π model etc. In this thesis it's again study these models for crosstalk noise estimation of two or multiple RC interconnects and compared with circuit simulation, for both noise peak and width estimation. It also estimates crosstalk noise in the presence of multiple aggressor lines correctly. This task is accomplished by comparing the crosstalk noise of different noise models. Unit step and saturated ramp input is used for aggressor which is present near the victim net. Then expression for noise peak and width has been derived and compared against simulation results and results are very promising. The results from 2π are better than the other models. The obtained noise amplitude average error of 2π model is (3.7%) which is lower than that from Devgan model (1558%), Heydari model (55.83%) and Vittal model (28.30%). So, the 2π crosstalk noise model is more appreciable for estimating the crosstalk noise for RC interconnects in deep sub-micron VLSI circuit.

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