



The Frequency, Time Design Analysis of Noise Figure Optimization of a Wideband PHEMT Hybrid LNA with Flat Gain for WiMAX Application

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ABSTRACT

In this paper, the Noise figure optimization circuit configuration in PHEMT Hybrid LNA design. The optimal noise figure is achieved by minimizing the noise contributions by utilizing of LC resonance at input and output matching networks to maintain transistor noise optimization. This article as added with not only frequency domain characteristics but also significant time response discussed. Design includes 2 stage cascaded common source PHEMT transistors with inter stage capacitor matching for improvement of gain. An LNA with Bandwidth 2.3-5.8GHz simulation in AWR Microwave office software shows forward gain of 24 dB, noise figure (NF) less than 2 dB and designed amplifier will give the best performance at 5GHz with NF of 0.9 dB and with flat Gain of 24dB. Furthermore, by balun structure input and output time analysis has been done by injecting sinusoidal sample signals with harmonic balance source models. Design is upgraded with EM structure mapping method for accurate results.

Keywords

Pseudomorphic High electron mobility transistor (PHEMT), Advancing in Wireless Evolution (AWR), Low Noise Amplifier (LNA) and Noise Figure (NF).

1. INTRODUCTION

LNA design is a crucial and challenging task at the receiver since received signal will always be weaker in amplitude and corrupted by noise in wireless communications. It should provide low noise figure not only at one frequency but an over range of frequencies or bandwidth of interest [1]. Also requirements of minimum noise figure and maximum gain will always be design trade-offs and cannot be met simultaneously. We need an optimization and fine tuning of component values to get the optimum results. For radio astronomy applications, it is desirable to have wider bandwidth, low noise figure and good gain. There is a trade-off between gain, bandwidth and noise figure (NF). High electron mobility transistor (HEMT) plays a crucial role and is extensively used in ultra-low noise amplifiers

2. A brief Review of existing wideband LNA with noise optimization

The key idea of proposed LNA is to get very flat gain throughout the band with minimum noise figure in order to verify and simulating the results AWR Microwave office is

used. In this paper [2] SheryAsaadWahbaMarzouk CS topology achieved a high gain but it has tradeoff between gain and matching but CMOS technology offers NF up to 3dB. So for the proposed design as FET technology is used and [3] Ahmed H DC, has tested in microwave the noise performance of GaAs mHEMT and InP pHEMT transistors were presented for both room and cryogenic temperatures by this result the proposed work as done on PHEMT transistor. [4] the inductive peaking technique is used to achieve high and flat value for S21 and good phase linearity is achieved and design include both cascade and cascode. In this paper [5] Pramod K B as simulated the LNA design with I/O matching and intermediate matching network in AWR Microwave office. So proposed work introduced 2 stage cascaded common source PHEMT transistors with I/O matching and capacitive intermediate stage matching networks.

3. Manufacturing Technology, Models and RF Performance Models

With the industry's most comprehensive and innovative portfolio of process technologies, E-PHEMT technology with a revolutionary chip scale package Transistor: GaAs pHEMT "ATF36163" from Avago technologies passive fitting to S parameter, EM multiple extraction, normal grounding type. A capacitor of 1pF value of Johansson Company was chosen and resistors of 1kΩ and 150Ω of Panasonic Company were chosen. The use of 0.25-micron gates allows an ultra-low noise figure with respectable associated gain. The PCB board material stack used to qualify the device consists of 40 mil thickness FR4 core material with one-ounce copper for both top and bottom metal.

4. Architecture Circuit design concept

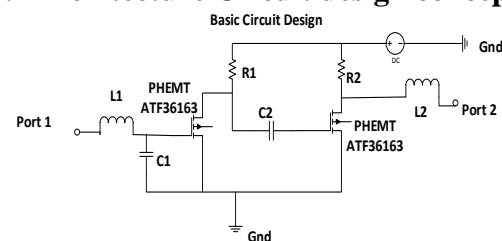


Fig 1: Basic circuit design with ideal elements without using micro strip line.

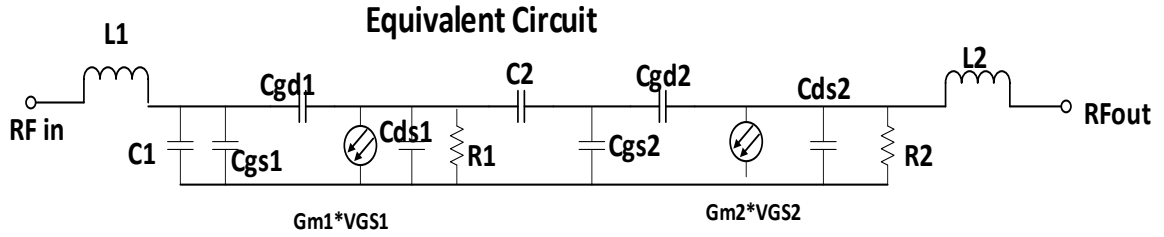


Fig 2: Circuit with necessary PHEMT model for realization.

$$Z_{in} = S_{L1} + \frac{1}{sC_{in}} \quad (1)$$

$$C_{in} = C_1 + C_{gs1} + C_{gd}(1 - Av) \quad (2)$$

Gain equations with respect to 2 stages

$$Av = Av1 * Av2 \quad (3)$$

$$Av1 = gm^* 1Z_{L1} \quad (4)$$

$$Av2 = gm^* 2Z_{L2} \quad (5)$$

$$gm^* = gme^{-i\omega\tau} \quad (6)$$

$$\tau = \frac{Cg}{gm} \quad (7)$$

$$gm = \frac{\epsilon_r \cdot V_{eff}}{d_{eff}} \cdot w_g \cdot \frac{1}{\sqrt{1 + \left(\frac{n_c}{n_{sheet}}\right)^2}} \quad (8)$$

Where,

gm = transconductance

ϵ_r is the relative dielectric constant

V_{eff} the effective carrier velocity, w_g the gate width,

d_{eff} an effective gate-to-channel separation

n_{sheet} is the sheet charge density and

n_c a reference sheet concentration defined as:

$$n_c = \frac{E_{crit} \cdot l_g \cdot C_0}{q} \quad (9)$$

E_{crit} is a critical field for the onset of a "saturated" behavior and C_0 is an effective channel capacity assuming a fixed distance between channel charge and gate in a simple capacitor model.

5. LNA Simulation with Vendor Components

5.1 Single Transistor

The stability factors of the transistor ATF-36163 given by figure below were found out in the frequency range of 2.3 GHz to 5.8 GHz.



Fig 3: ATF-36163 transistor model

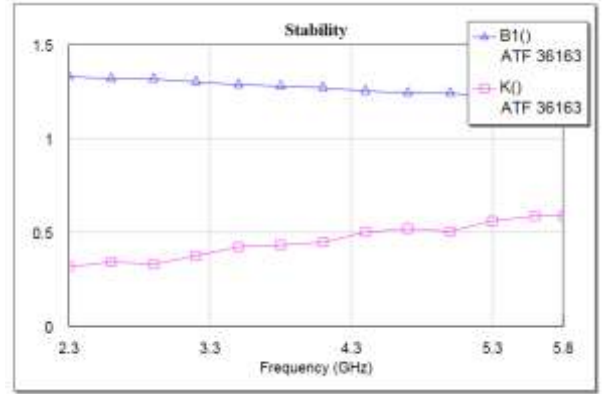


Fig 4: Stability graph of ATF-36163 transistor

The transistor is found to be unstable and gain of the transistor is varying from 13 dB to 12 dB in the desired frequency range but we want to achieve a gain of greater than 20 dB, thus we have cascaded two transistors.

5.2 Two Transistors in cascade

Two transistors, ATF-36163 were connected in cascade as shown in figure 5, and the forward gain (figure 6), stability parameters (figure 6) were calculated again in the frequency range of 2.3 GHz to 5.8 GHz.

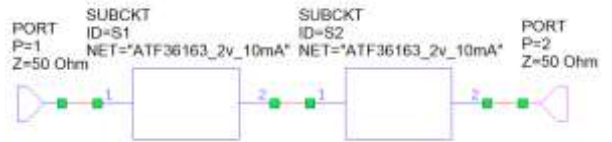


Fig 5: Schematic of Two Transistors in Cascade

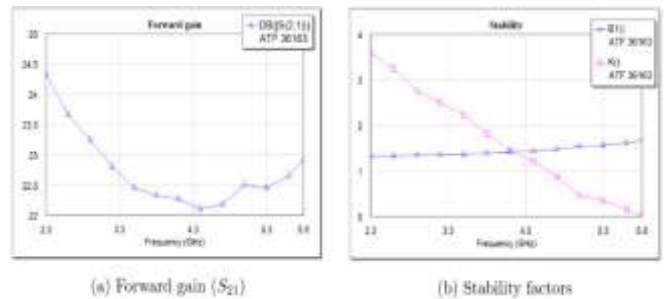


Fig 6: Results of Two Transistors in Cascade

The forward gain S_{21} was found out to be greater than 20dB, but the sub circuit was found to be unstable. Thus it was necessary to stabilize the sub circuit.

5.3 Stabilized Sub-circuit

The schematic of the stabilized sub-circuit (figure 7) is given below

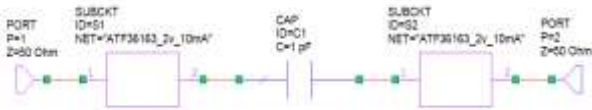


Fig 7: Stabilized sub-circuit schematic

The stability factors (figure 8), $K > 1$ and $\beta > 0$, were satisfied for the stabilized sub-circuit in the frequency range of 2.3 GHz to 5.8 GHz.

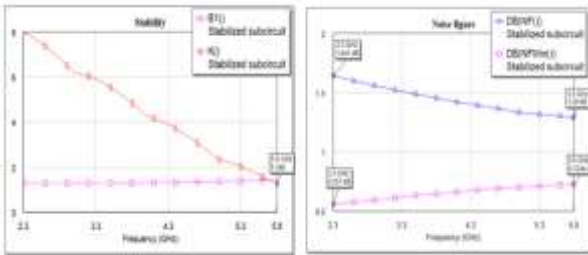


Fig 8: Figure Stability of Stabilized Sub-circuit and Noise figure of Stabilized Sub-circuit

5.4 DC Biasing

One of the major advantages of the enhancement mode technology is that it allows the designer to be able to dC

ground the source leads and then merely apply a positive voltage on the gate to set the desired amount of quiescent drain current I_d .

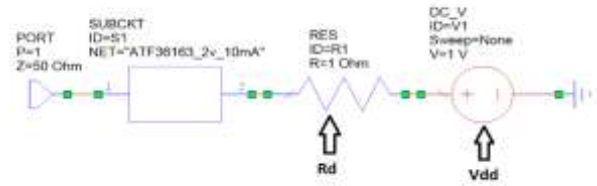


Fig 9: DC Biasing

Applying KVL in the output loop we get the following equation:

$$V_{DD} - I_D R_D - V_{DS} = 0$$

Here $V_{DD} = 12V$ and I_{DD} is 10mA, using this values we get the value of R_D as 1K Ω .

5.5 Intermediate LNA Schematic

After obtaining the biased sub-circuit, the micro-strip lines are added to connect the lumped elements. Following micro strip lines were then added: “Mlins”, “Mtees”, “Mtaper” etc. After adding micro strip lines, the ideal capacitors and resistors were replaced with industry available components.

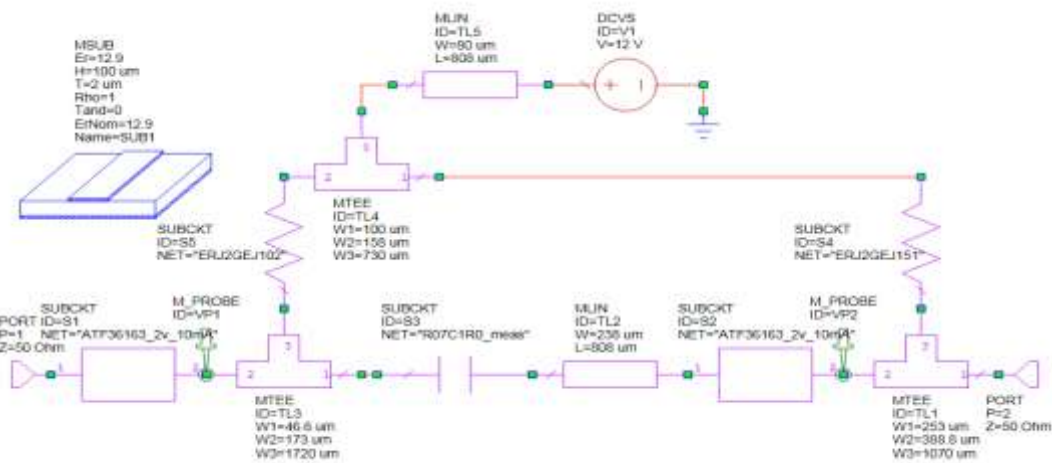


Fig 10: The final intermediate schematic design

The substrate with $\epsilon_r = 12.9$ was selected. As we go on increasing the permittivity of the substrate the thickness of the substrate goes on decreasing without causing any complications in the functioning of the circuitry.

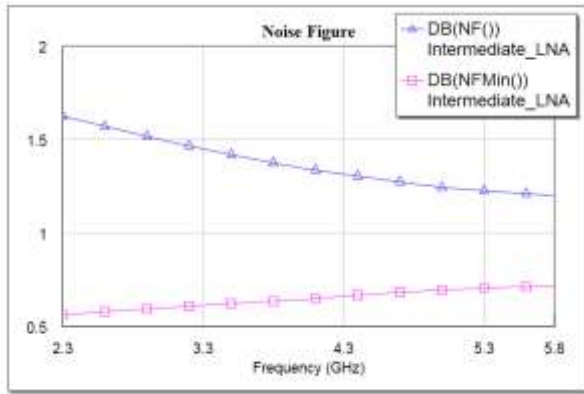


Fig 11: Noise Figure of Intermediate LNA

The DC current (I_{DS}) and DC voltage (V_{DS}) are as follows:

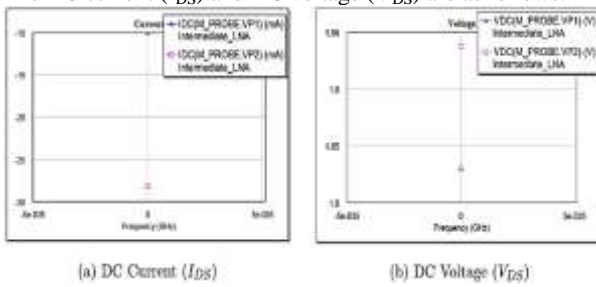


Fig 12: DC Current and Voltages

6. Matching Networks

The techniques for impedance matching an enhancement mode device are very similar to those for matching a depletion mode device. The matching network (figure 13) consists of matching networks at input and output ends of the intermediate circuit.

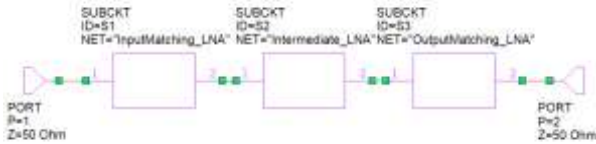


Fig 13: Matching network

The matching equations are,

$$G_{Tmax} = G_{Smax} * G_O * G_{Lmax}$$

$$G_{Smax} = \frac{1}{1 - |S_{11}|^2}$$

$$G_O = |S_{21}|^2$$

$$G_{Lmax} = \frac{1}{1 - |S_{22}|^2}$$

6.1 Input Matching

For input matching, in general the block before LNA either antenna or filters which is connected will have standard characteristics of 50Ω output resistance. In order to lower the system noise and to ensure the maximum power transfer should have zero reactance.

The source gain circle equations are:

$$g_s = \frac{G_s}{G_{Smax}}$$

$$C_{gs} = \frac{g_s * S_{11}^*}{1 - |S_{11}|^2(1 - g_s)}$$

$$R_{gs} = \frac{\sqrt{1 - g_s}(1 - |S_{11}|^2)}{1 - |S_{11}|^2(1 - g_s)}$$

Where,

C_{gs} = center of the source gain circle

R_{gs} = radius of the source gain circle

The noise circle equations are:

$$N = \frac{(F - F_{min})(1 + |\Gamma_{opt}|^2)}{4R_n}$$

$$C_F = \frac{\Gamma_{opt}}{N + 1}$$

$$R_F = \frac{\sqrt{N^2 + N(1 - |\Gamma_{opt}|^2)}}{1 + N}$$

Where,

C_F = center of the noise circle

R_F = radius of the noise circle

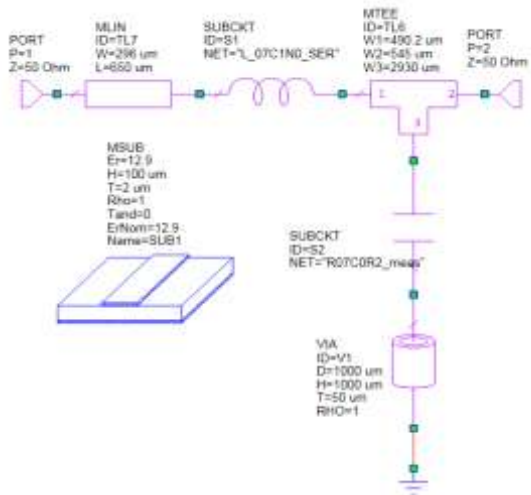


Fig 14: Schematic of Input Matching Network

6.2 Output Matching

For output matching,

The load gain circle equations are:

$$g_L = \frac{G_L}{G_{Lmax}}$$

$$C_{gL} = \frac{g_L * S_{22}^*}{1 - |S_{22}|^2(1 - g_L)}$$

$$R_{gL} = \frac{\sqrt{1 - g_L}(1 - |S_{22}|^2)}{1 - |S_{22}|^2(1 - g_L)}$$

Where,

C_{gL} = center of the load gain circle

R_{gL} = radius of the load gain circle

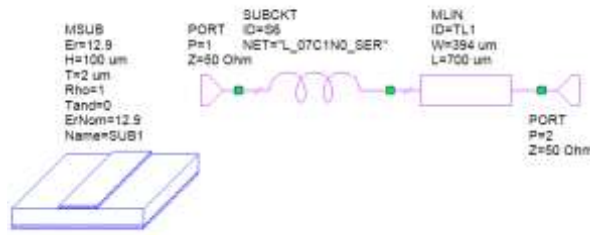


Fig 15: Schematic of Output Matching network

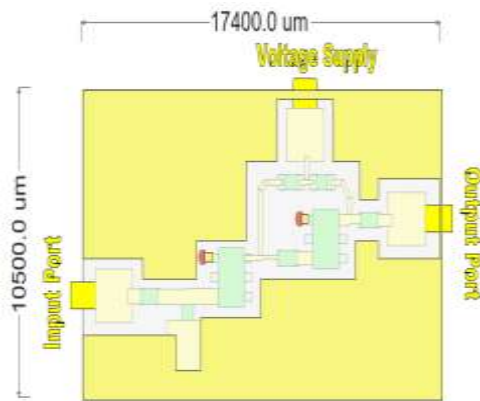


Fig 16: 2D View of LNA

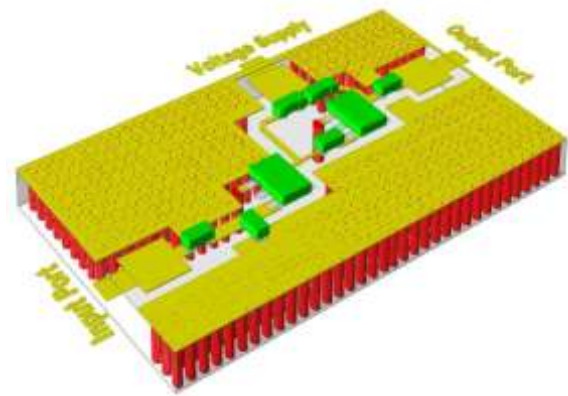


Fig 18: 3D View of LNA

The red cylinders are vias. The green components are lumped circuit elements. The yellow patches are copper patches

7. Complete LNA Design

After combining Input Matching circuit, Intermediate sub-circuit and Output Matching circuit into a single circuit, the low noise amplifier was designed.

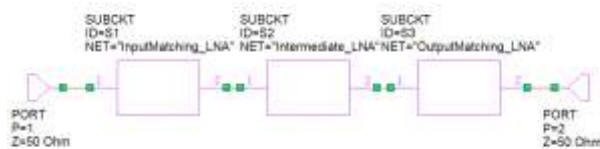


Fig 17: Schematic of Complete Low Noise Amplifier

7.1 Development of Layout

Layout is facet of the LNA design work will all vendor components is complete and errors have been successfully removed with the additional steps process: Extraction, Layout Versus Schematic (LVS) Check, and Post-Layout Simulations. Extraction involves the creation of a circuit description called a netlist which provides information regarding the transistors and their interconnections. The circuit is terminated with a 50Ω port on the input and output side. The circuit is named LNA

8. Simulation Results and Analysis

8.1 The forward gain (S21)

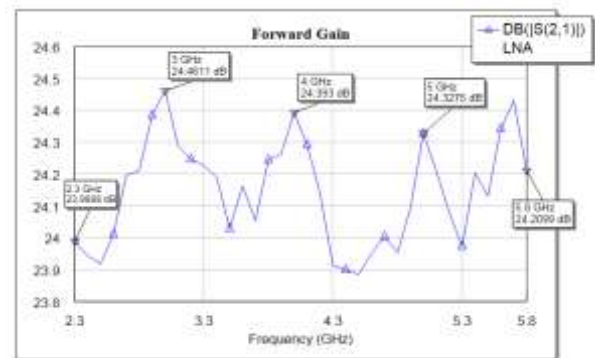


Fig 19: Forward gain response of the complete circuit.

The forward gain (S21) of the LNA varies from 23.89 dB to 24.46 dB in the frequency range of 2.3 GHz to 5.8 GHz while providing a flatness of 0.57dB. The forward gain takes a maximum value of 24.46 dB at 3 GHz and is considerably high at 4 GHz and 5 GHz.

8.2 Noise Figure (NF)

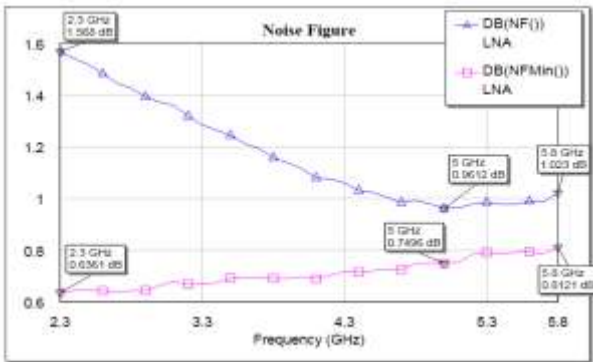


Fig 20: Noise figure response of the complete circuit.

The noise figure (NF) goes on decreasing with the increase in frequency from 1.56 dB at 2.3 GHz to 1.02 dB at 5.8 GHz, and has the minimum value of 0.96 dB at 5 GHz. The minimum noise figure goes on increasing as the frequency increases from 0.63 dB at 2.3 GHz to 0.81 dB at 5.8 GHz.

8.3 Return Loss

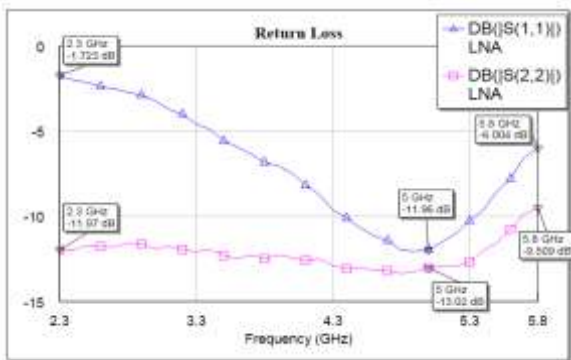


Fig 21: Return loss of the complete LNA circuit.

The input return loss S11 is less than 0 dB throughout the frequency range of 2.3 GHz to 5.8 GHz and is minimum at 5 GHz with -11.96 dB value. The output return loss S22 is less than 0 dB throughout the frequency range of 2.3 GHz to 5.8 GHz and is minimum at around 5 GHz with -13.02 dB value.

8.4 VSWR Limitation

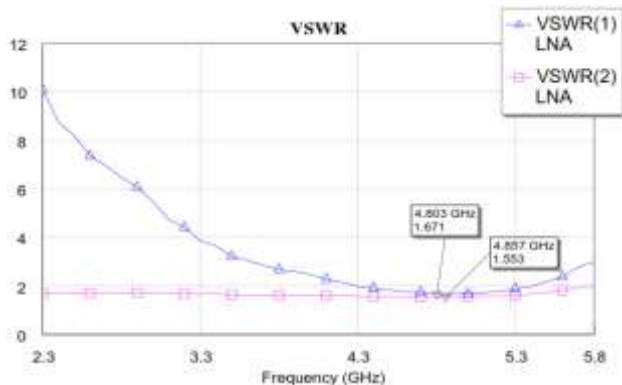


Fig 22: VSWR at Input and Output of the complete LNA circuit.

Design shows very good response at 4.8GHz at input side 1.6 and output side 1.5GHz and there is small limitation at the input since its value is more at lower frequency and optimum value after 3.5 GHz.

9. Time domain analysis

for the time analysis to the designed LNA primary requirement to visualize the coaxial cable effects with the input and output port balun structure are used.

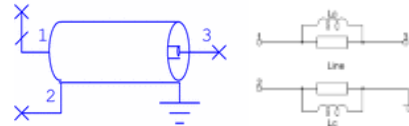


Fig 23: Symbol and equivalent circuit for Balun.

This balun model is a balanced-to-unbalanced transformer which consists of a transmission line wound around a ferrite core. The external balanced line connects to ports 1 and 2; the external unbalanced line to port 3. The choking inductance, L_c , is

$$L_c = \mu_u \cdot L \cdot LEN$$

Where, L is the inductive index, LEN is the physical length of the transmission line.

The attenuation A(F) has the following frequency dependence:

$$A(F) = \begin{cases} AF = 0 \\ A(F) \cdot \sqrt{\frac{f}{F}} & F > 0 \end{cases}$$

where f is a simulation frequency.

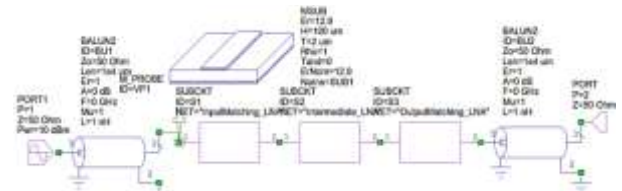


Fig 24: complete design is excited with 1 tone HB source.

the complete circuit is excited with 1 tone Harmonic balance source with fundamental frequency up to 10dBm at the input side and other end is terminated.

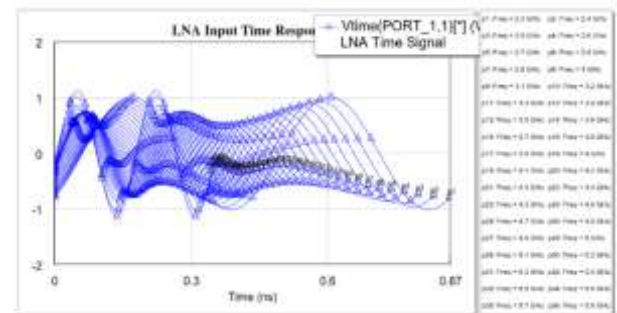


Fig 25: Time signal analysis at the input port 1.

The above resulted figure is the response when the active circuit is excited with 1 tone HB with the frequencies 2.3GHz to 5.8GHz with step of 0.2GHz.

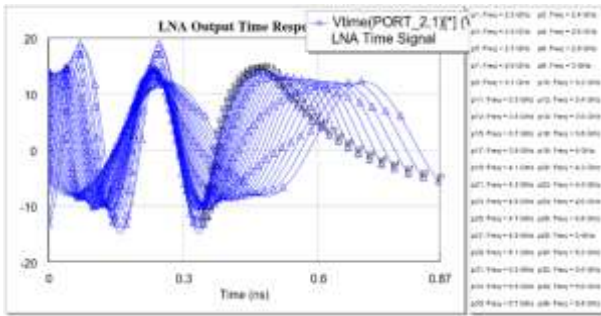


Fig 26: Time signal analysis at the output port 2.

The above resulted response is found when the active circuit is excited for the active termination that applies load impedance $Z(50\Omega)$ while supplying a power signal of magnitude power and angleswept across the band (2.3GHz to 5.8GHz).

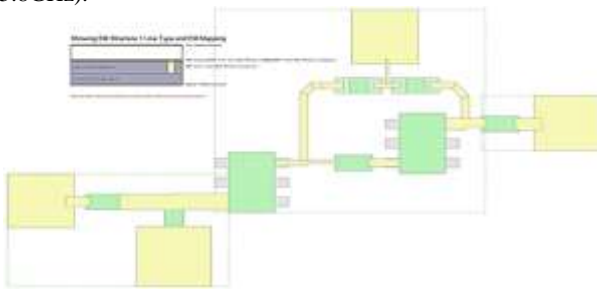


Fig 27: Showing EM structure line type with EM Mapping layout.

The design is updated to EM structure line type with EM mapping which uses both physical properties and conduction properties in stack up. It has been re-simulated for the entire frequency band. Each and every sub block have been updated with new interpolation data and extrapolation was not possible for this design.

10. Conclusion

At the system level, receiver sensitivity is dominated by the noise figure, Gain and linearity so in this paper a two stage LNA is designed by adding an input and output matching Network and DC bias, its behavior is carefully analyzed in AWR Microwave office. An algorithmic design methodology for simultaneous noise and input/output impedance matching in Microwave LNAs has been presented and verified. The results achieved in this work is having I/O matching network which is evaluated and relative performance is compared with below mentioned papers in terms of bandwidth, forward gain and noise figure.

Table 1. Comparison between proposed work and related recent published work

Reference	Bandwidth (GHz)	Noise Figure (dB)	Gain (dB)
[6]	Single point at 1	0.6	17.49
[1]	2-11	1.6-4	15
[7]	Single point 2.4	1.8	12.09
[8]	2.1-2.5	1.9-2.1	11.9
This work	2.3-5.8	<1.5	24
This work	5	0.9	24

Thus, the designed amplifier has claims the advantages of better matching network yields a Forward flat gain of 24 dB Noise figure less than 1.6 dB over the bandwidth from 2.3

GHz to 5.8 GHz with high linearity and stability. The design shows the best performance at 5GHz providing the Gain 24dB and limiting the Noise figure to 0.9dB. The design is thoroughly measured by using harmonic balance models. Time analysis has been executed at both input and output ports with 1 tone analysis. For time analysis the excited tone has been varied from 2.3GHz to 5.8GHz with RF input up to 10dBm. The design has got very compromising response with sinusoidal signal and also in turn promising for random signals too. Design is upgraded with EM Structure mapping which is very much required for all microwave device which operates more than 2GHz.

11. Future scope

In future multilevel interconnects to realize vertically integrated RF, Microwave MMIC technology is expected to use the current Hybrid technology design. So this work as opened numerous area for future work with respect to flat gain response in LNA design which could be done better understanding for the LNA measurements in the receiver system. The shown 3-D layout technology and EM Structure mapping is promising in performance of fabrication. Same design can be upgraded to MMIC design by using Industrial standard process development kit. The MMIC fabrication techniques are diffusion, ion plantation and epitaxial growth etc. required this kind of work on basic hybrid MIC technology. In addition to this work followed by the fabrication by using MMIC technology and will be integrated to the receiver system of some of the applications like WiMAX, Digital Audio Radio Satellite (DARS), Amateur radio, Airport surveillance radars and S/C band radars. Also commercially viable wireless application in huge scale.

12. ACKNOWLEDGMENTS

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14. AUTHOR PROFILE

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