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Digital Front-End for Software Defined Radio Wideband Channelizer

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ABSTRACT
This paper focused on the design of a digital front end channelizer useful in most software defined radios with the aim of exploiting the vast resources of digital signal processing which helps to achieve a portable, long lasting with extraordinary computational complexity software application that is capable of running at a lower power budget. Three channelization algorithms: per-channel, pipeline frequency transform and poly-phase fast Fourier transform uniform channelization algorithms were reviewed and designed for FM receivers using Altera Digital Signal Processing tool box in MATLAB/Simulink environment. The performance evaluation of the three algorithms were carried out with the estimation of the multiplication per input samples of operation of the system, signal strength level or signal to noise ratio and the compilation time of each algorithm. The result showed that the polyphase fast Fourier transforms and pipeline frequency transform had 24% decrease in computational requirement compared to per-channel which suggest a lower power consumption. Whereas, polyphase fast Fourier transform out performs pipeline frequency transform in terms of silicon cost.

General Terms
Algorithms, Fast Fourier Transform, Digital Signal Processing, Software Defined Radio, Digital Front End.

Keywords
Channelization, Multirate Digital Filter Bank, Software Defined Radio, Digital Down Conversion.

1. INTRODUCTION
The digital front end section of Software Defined Radio (SDR) receiver system is one of the recent research areas in communication engineering which as well has found application in many other fields such as smart systems in power engineering **[7]**. The most important reasons for such system are: ability to easily incorporate with multi- media functionalities, interface with other digital devices, compute at a reasonably fast speed depending on the system channelization architecture **[1,9]**, support multiple protocols, prototype and fix bugs for next generation protocol implementation **[14]**. The practical application of the SDR, as made evident in telecommunication stations, include: Global System for Mobile Communication (GSM): 2G/ 3G/ 4G radio, IS-95, Universal Mobile Telecommunication Standard (UMTS), radio and television broadcast for commercial and military use **[8,13]** and are characterized with different center frequency, channel bandwidth, noise level, interference requirements, and transmit spectral mask.

The most important aspect of the SDR architecture is the software part which handles the digital signal processing of the digital front end which so far has incorporated different channelization algorithms both uniform and non-uniform to achieve an optimum system in terms of computation and efficiency. The wideband channelizer decomposes the digital Intermediate Frequency (IF) input signals into separate baseband output signals. Examples of major uniform channelization algorithms used are per-channel, pipeline frequency transform and poly-phase fast Fourier transform, while farrow structure filter bank is used for non-uniform algorithm. More specifically, the channelization technique is composed of the down-conversion and filtering of every communication channels followed by sample rate conversion (SRC) of each channel from a high sampling rate to a lower rate so that the baseband signal can be extracted at less computational complexity. The multirate multistage technique was also adopted to achieve an optimized channelization algorithm.

The digital section of SDR receiver receives IF wideband digital signal bandwidth from the ADC for complex baseband signals channelization. To reduce the high sample rate of the digital signal, an intermediate SRC is applied to extract channels up to the baseband signal bandwidth according to Nyquist criterion. These three (3) algorithms were simulated using Altera Digital Signal Processing (DSP) tool box in MATLAB/ Simulink environment for a proposed FPGA processor.

2. RESEARCH METHOD
The whole system is analogous to that of superheterodyne receiver architecture as shown in Fig 1. Based on this architecture, the RF analogue signal is been modelled based on available real FM channels by the use of MATLAB/ Simulink software. This RF signal enters the receiver through the antenna which is either incorporated into the FPGA board or designed on an expandable circuit before its incorporation into the FPGA board. Instead of dealing with high dynamic ranges or requirements and sampling frequency required for the simulation of the RF signals based on Nyquist criterion in the radio frequency (RF) section of the radio receiver, the intermediate frequency (IF) is used which is derived from mixing the signal RF with a local oscillator signal of a given fixed/ variable frequency.

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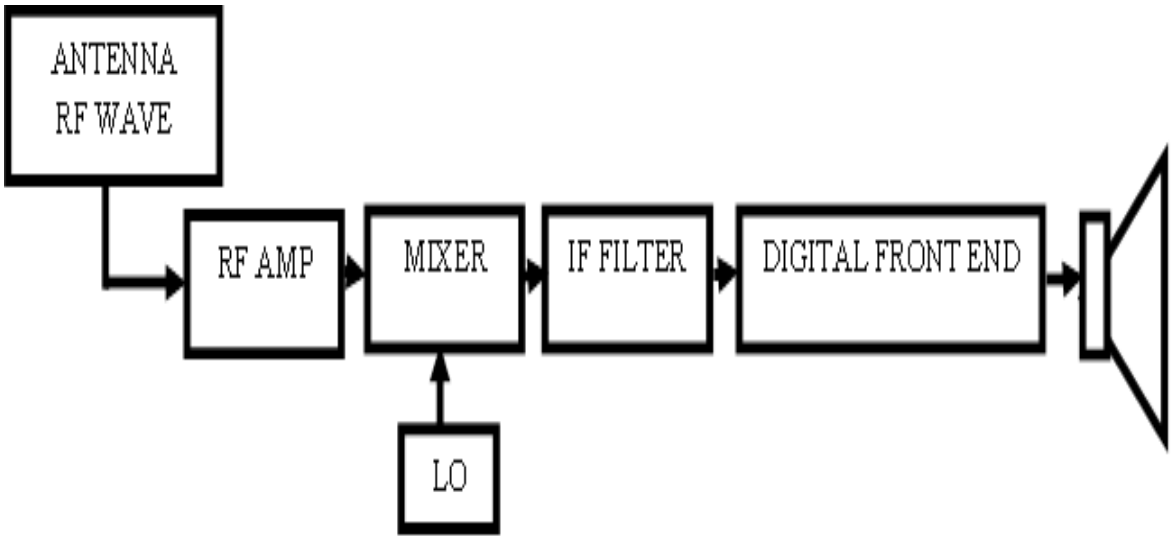

Fig 1: The block diagram of the super- heterodyne radio receiver

The IF obtained allows easy digitization of the signals by using an analogue to digital converter (ADC) capable of running at a sampling time of greater or twice the IF with maximum dynamic range of 100 MHz **[7]**. This is contrary to the direct down conversion of multiband RF to band pass signals as described by **[3]** where under sampling is used.

2.1 Signal Generation and Modelling

The communication signals are modelled to mimic real life radio systems, simulated in preparation for real life implementation. Considering an analogue passband FM signal, x(t), obtained when an audio signal input, u(t), mixes with a carrier signal, v(t), generated by a local oscillator (LO) at the transmitting end. An outcome is obtained which is a varied frequency of the carrier wave, $f_{c,}$ about a mean value as a function of the magnitude of the baseband audio frequency, $f_{a,}$ as shown in Figure 2.

$$x(t) = K_c \cos(2\pi f_c t + k_f \frac{K\alpha}{f_a} \sin 2\pi f_a t)$$

$$\Delta f = k_f * K_\alpha$$

$$\mu = \frac{\Delta f}{f_a}$$

where

f_c is the carrier frequency.
k_f is the modulation constant or index.
Δf is the frequency deviation, representing frequency variation from the carrier frequency.
μ is the phase deviation of the FM signal or the modulation index which has values from 1 to 5 **[12]**

The sample time for the audio signal or RF front end signal is taken as greater or equal to the inverse of twice maximum frequency of the FM range or the carrier frequency. The modulating signal specification as illustrated in the Table 1 is allowed to pass through frequency modulation scheme which shifts the baseband signal and centers it at passband (carrier frequency). Although in communication receiver application, the RF input at the antenna involves several channels of different carrier frequencies and amplitude in the presence of channel noise which are summed together.

Table 1: Modulating signal specification

Source	sine wave
Maximum audio frequency	15 kHz
Signal amplitude	1 (+27 dB)
Sampling time	2.5e-9

The requirements of sound quality for commercial radio stations require a bandwidth of about 15 kHz (Table 1).

The Carson's rule was used to estimate the available channel bandwidth needed to avoid channel interference as expressed below which shows that for FM radio broadcasting, the allocated channel band-width is approximately 200 kHz.

$$\text{Channel spacing bandwidth} = 2\ (f_{dev} + f_{max})$$

where f_{dev} is the maximum frequency deviation (75 kHz)
f_{max} is the highest base band signal frequency (15 kHz)

Gaussian noise channel added to the sum of FM signals obtained a signal to noise ratio (SNR) of approximately 20 dBm. The gaussian noise used generates discrete-time white noise which is random over the passband frequency spectrum. This normalizes the noise level about a mean of zero dBm point over the passband frequency.

2.2 Analogue Front End Design

The analogue front end section of a radio receiver also called the RF section describes the operation of the low noise amplifier (LNA), and the demodulation section. The signal incident to the antenna is of small magnitude (i.e. weak signal strength) because of the presence of noise in the channel which will be compensated for with the RF amplifier but in any case it will be received by the receiver. The RF amplifier forms one of the analogue front end components which provides initial gain and selectivity and minimizes radiation of

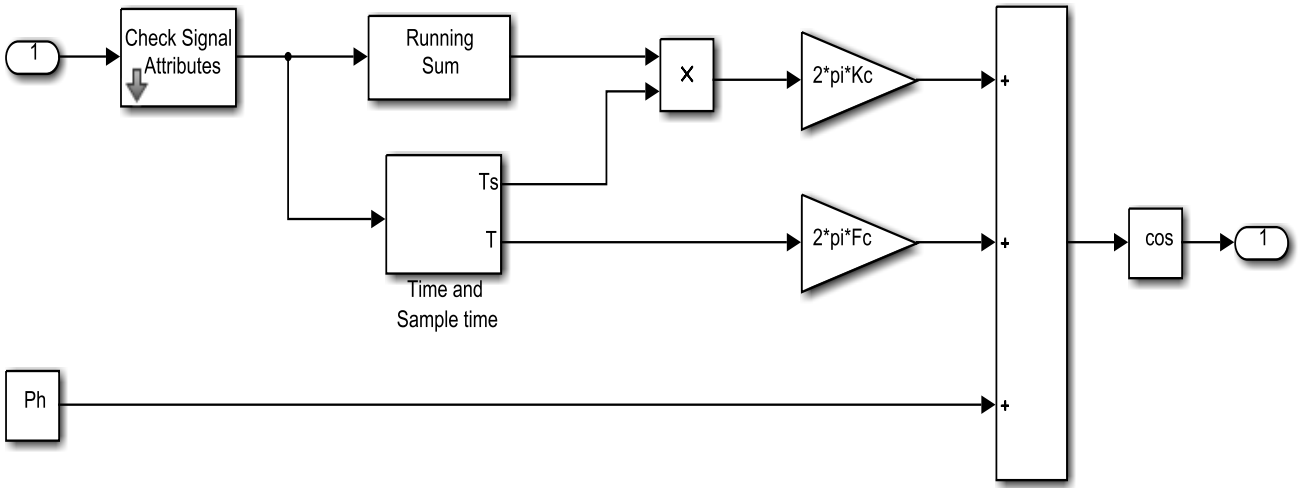

Fig 2: Internal structure of a Frequency Modulator in MATLAB/ Simulink

the local oscillator and also helps to eliminate image and noise frequencies.

The LNA block in the MATLAB/ Simulink environment is obtained from the Simscape library which requires input, output port and the RF configuration block as illustrated in Fig 3. These ports are used to specify the input and output impedance matching from the antenna to the LNA and from the LNA to the mixer, which is usually 50 ohms.

The other requirements for LNA in most communication system is that the noise figure must be less than 3 dB and also the gain must have at least noise figure plus 10 for the device to pick up the signal over its internal generated noise **[5]**. In the design the following requirements were used as shown in Table 2.

Table 2: LNA design requirements

Input and output impedance	50 Ω
Max input carrier frequency	108.1 MHz
LNA gain	20 dB
Noise figure	2
IP2 and IP3	Infinity
Output signal	Real passband (88.1 MHz to 108.1 MHz)

The incoming carrier signal frequency components of FM are observed to be high compared to the speed/sampling frequency of most ADCs used. Therefore, analogue signal frequency shift to a lower frequency band is required.

The local oscillator signal is represented with real cosine wave having sampling time as the RF signal.

$$f_{LO} = f_{RF} \pm f_{IF}$$

The presence of image frequency which has signal frequency greater than the LO frequency mixes with the LO frequency to give a mixer output equal to the IF.

$$f_{image} = f_{RF} + 2f_{IF}$$

The intermediate frequency (IF) design stage is characterized with multi- harmonics obtained by the frequency sum and difference between the received signal and the local oscillator signal **[2]**. The difference frequency IF is one important output frequency used in the design process, which is the frequency ranging from 10.7 MHz to 30.7 MHz.

The purpose of the design is to replace all analogue components with digital components. Therefore, the low pass filter required at the IF end is preferably a digital low pass filter which must convolve with a discrete IF signal. Besides, all channelization tasks are performed digitally; in other words, there must be a signal conversion from analogue to digital which requires a rate converter from the initial sampling rate of 400 MHz to 64 MHz which is placed immediately after the mixer output.

2.3 Digital Front End Design

The analogue to digital conversion procedure involves the conversion of continuous time signals into a discrete time signal at instant multiples of the sampling interval T_s and can be expressed in three steps

a. Sampling
b. Quantization
c. Coding

Quantization step of the ADC can be expressed as:

$$\alpha = \frac{V_{fs}}{2^B - 1}$$

where V_{fs} is the full scale peak voltage
α is the quantization step or resolution
B is the bit of the ADC

Therefore the Quantization signal to noise power ratio is given as:

$$S/N = \frac{\frac{{V_{fs}}^2}{2}}{\frac{\alpha}{12}}$$

In decibel, the ideal form of signal to noise ratio is given as

$$SQNR\ (dB) = 1.76 + 6.02B$$

According to **[4]**, the quality of the output of the ADC is usually measured by the signal to quantization noise ratio, which is the ratio of the signal power to the noise power. The ADC for receiver requires 100 dB or more for the dynamic range characteristics and the higher the bit (B) of the ADC, the better the resolution of the signal been digitized.

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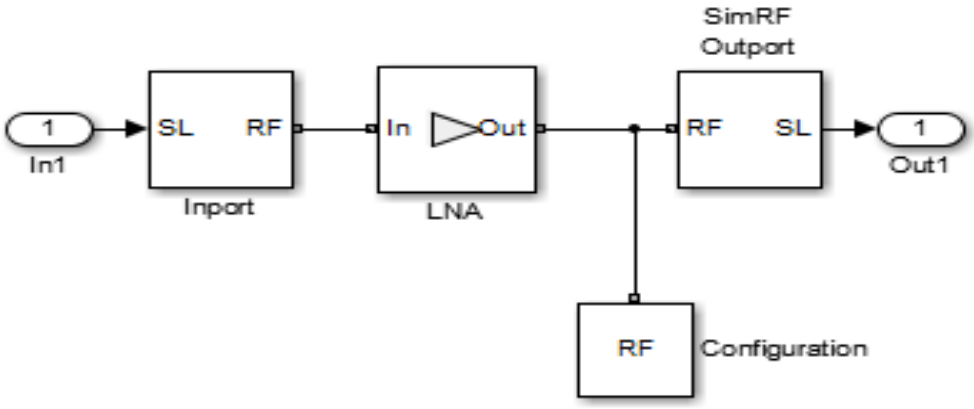

Fig 3: Block diagram illustrating LNA design

This digitized signal has a frequency of 10.7 MHz corresponding to the IF of commercial FM broadcast station. It is important that the ADC be sampled based on Nyquist criterion *fs ≥ 2*fm* which helps to remove aliasing or signal distortion. This justifies the use of sampling rate of 64 MHz for the simulation.

The discrete data is obtained by multiplying the input signal, $x_c(t)$, with a Dirac delta function $\delta(t\text{-}nT_s)$ at specific intervals as shown in Figure 4 **[15]**.

As $\delta(t\text{-}nT_s)$ is 1 at $t\text{-}nT_s = 0$ and otherwise 0, the attained signal is: $x[n] = x_c(t - nT_s)$

$$x[n] = \sum_{k=-\infty}^{\infty} x(k)\,\delta(n-k)$$

The output of the ADC (discrete IF signals) is then convolved with the low pass digital filter frequency response to eliminate the sum IF. The response of the system to x[n] is the corresponding sum of weighted outputs, y(n), therefore

$$y(n) = \tau(x[n]) = \tau\left[\sum_{k=-\infty}^{\infty} x(k)\,\delta(n-k)\right]$$

$$= \sum_{k=-\infty}^{\infty} x(k)\,\tau[\,\delta(n-k)]$$

$$= \sum_{k=-\infty}^{\infty} x(k)\,h(n-k)$$

This illustrates a finite causal system with finite numbers of delays which connotes a finite number of storage locations to be practically implemented. The MATLAB/Simulink implementation of the FIR filter involves using the digital filter design and analysis toolbox (FDATool) characterized with a linear phase in the pass band region with the aim of suppressing or attenuating all other possible signals in the stop band region. Based on the design specifications, two different filter configurations were observed. The first having a bandpass equiripple filter of minimum order which allows only digital signals of 10.7 MHz to pass while it attenuates the other frequency. This convention allows system control of individual channels from the local oscillator in the analogue front end. At the output of this filter only a single NCO is required which mixes the signal to baseband. The multirate multistage down sampling filters helps to filter out the high frequency while retaining the baseband signal as well as reduce the sampling rate.

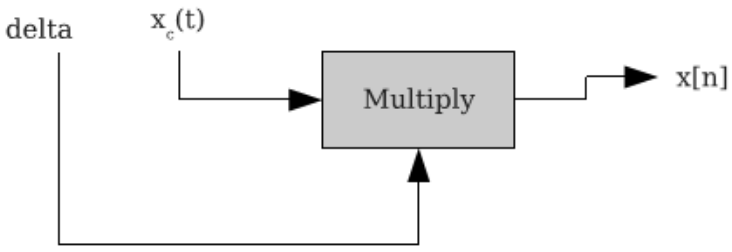

Fig 4: The Discrete Data Representation of the Continuous Signal [15].

The second configuration utilizes also a bandpass equiripple filter of minimum order which allows signals within the range of 10.7 MHz and 30.7 MHz to be selected while attenuating all other frequencies. This configuration was adopted in the channelization algorithm design since multiple channels are needed to be extracted within the frequency range therefore, a digital control NCO is needed for such implementation. The sampling frequency of the filter is 64 MHz with a stop band attenuation of 60dB.

The digital down converter (DDC) is an important section in any digital radio which performs frequency translation from 10.7 MHz to baseband at a high input sample rates. The convolved output of the input digital signal and the digital

filter mixes with a numerical controlled oscillator (NCO) signal having a frequency f_{LO} of 10.7 MHz and sampling rate of 64 MHz to generate a sine, cosine or complex wave.

$$f_{NCO} = f_{BB} \pm f_{IF}$$

The NCO is capable of generating a multichannel real or complex sinusoidal signal depending on a real input IF signal. These NCO signals have independent frequency and phase in each output channel with amplitude equal to 1.

The output NCO block allows the adder's numeric values to overflow and wrap as shown in Fig 5. The lookup table is constructed from a double precision floating point values with maximum amount of precision output of 53 bits.

Fig 6 illustrates a 10.7 MHz NCO signal generated. At the output of the mixer two frequencies were generated but, the one that interest the designer is that centered at 0 Hz. The presence of a low pass filter at the output of the mixer helps to eliminate frequency at 21.4 MHz and above.

2.4 Digital Rate Conversion Design

Based on the fact that the transition bandwidth (ΔF) of the baseband signal is small compared to the sample rate fs (64 MHz) therefore to realize a filter to this precision, the order of the filter or number of coefficients is increased. In order to process this large number of coefficients with considerable word length processing and clock rate for a single channel filtering in a direct implementation by means of a conventional FIR filter, a lot of effort and high cost of multipliers would be required. To overcome this, a lowpass filter which does channel filtering on the baseband signal is combined with a down sampler (decimation) in a multi-stage pattern **[11]**.

The multi stage decimation factor is such that it is not a prime number that is, it can be written as a product of individual decimation factors ($M=\Pi m_i = m_1 * m_2 * \ldots m_k$).

The total decimation factor can be calculated as:

$$M = \frac{fs_{inp}}{fs_{out}}$$

where fs_{inp} is the input sampling frequency from the ADC (64 MHz)

fs_{out} is the desired sampling frequency for the output signal (250 kHz).

The desired sampling frequency (250 kHz) is a function of the channel spacing of the FM spectrum (0.1 MHz) in which according to Nyquist criterion should be twice the channel spacing. The total decimation factor equals 256.

The oversampling ratio (OSR) of the signal, which is the ratio between the sample rate, *fs*, of the signal and the band width (ΔF) of the signal of interest, is typically high in the first few stages of the multirate filter as a result of a large transition band and narrow stop band. A comb filter which is sufficient enough to attenuate the narrow stop band is employed.

The cascaded integrator comb filter (CIC filter) transfer function is expressed below:

$$H(z) = \left(\sum_{i=0}^{M-1} z^{-i}\right)^R$$

$$H(z) = \left(\frac{1 - z^{-M}}{1 - z^{-1}}\right)^R$$

where M is the sample rate reduction factor and R is the order of the CIC filter.

The CIC is the first decimation block with flexible multiplier free filter suitable for hardware implementation that can handle arbitrary large rate changes. This CIC is made from a cascade or chain of an integrator and comb filter. The comb filter requires no multipliers, but uses adders, subtractors and registers. The filter is also known for performing high decimation sufficient to 4-times of the Nyquist rate according to *Hogenauer* **[6]**. A single stage integrator is expressed as:

$$y[n] = y[n-1] + x[n]$$

The comb filter runs at the same high sampling rate for a given rate change M which is an odd symmetric FIR filter and a single stage comb is expressed as:

$$y[n] = x[n] - x[n-RM]$$

where R is called a differential delay which can be any positive integer, but it is usually limited to 1 or 2 still at the sampling rate *fs*.

When R and M equals unity, the power response depicts a high pass function with 20 dB per decade which is an inverse of an integrator. When RM $\neq$ 1, the power response show similarities with the raised cosine form which has its RM cycle from 0 to 2π. In MATLAB/Simulink implementation, the CIC filter block was selected from the DSP system Toolbox. The CIC decimation factor (m_1) was calculated to be 64 by using the formula below:

$$m_1 = 2M\frac{\left(1-\sqrt{\frac{M\Delta F}{2-\Delta F}}\right)}{2-\Delta F(M+1)}$$

where ΔF = transition frequency and M is the overall decimation factor. The differential delay was set to 1 and the passband frequency as 0.1 MHz at a stopband attenuation of 60 dB.

In all the three algorithms studied, the CIC filter is common to all. The per-channel algorithm, after the CIC utilizes a direct form inverse sinc FIR lowpass single rate filter after which it is down sampled by a factor of 4. This low pass filter helps to compensate for the pass band drop caused by the sinc-like response of the CIC. The polyphase concept is used in the pipeline frequency transform channelization algorithm, only that it is in an hierarchical form which uses the inverse sinc and the final lowpass filter each decimated by 2 as in polyphase fast Fourier transform channelization algorithm

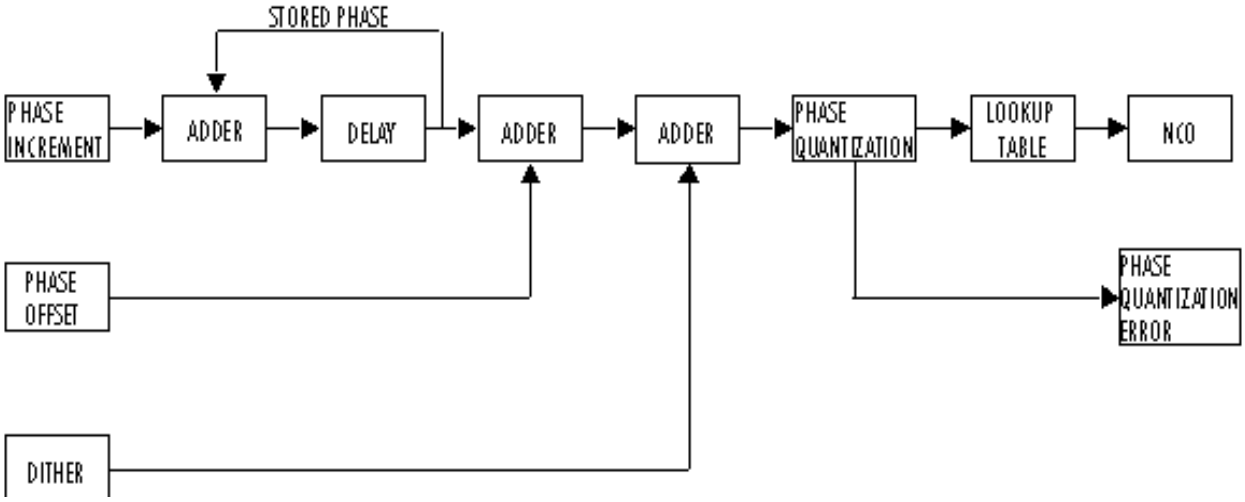

Fig 5: Internal structure of NCO in MATLAB/Simulink

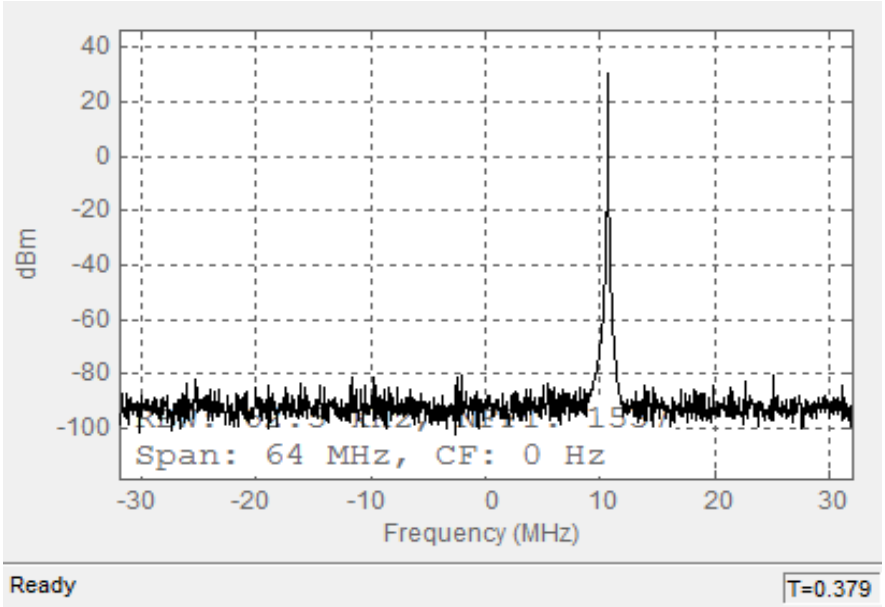

Fig 6: Spectrum illustrating a 10.7 MHz output NCO signal

2.5 Polyphase Decimation

The polyphase decimation approach introduces a more efficient way of representing the multistage rate conversion filters. This allows filter output samples that are necessary to be retained where others are discarded.

In order words, a signal that is down sampled by a factor M will have M different phasing alignments between the filter output samples with respect to the filter coefficient **[10].**

Given an M -1 decimator, with a filter response of h(n). The filter only computes the outputs: y[0], y[M], y[2M], … where we observe that y(n) is a product of x(n) and h(n). Therefore, it follows that the input signal can be split into M separate sequences

$x_0(n) = \{x[0], x[M], x[2M]\ldots\}$

$x_1(n) = \{x[1], x[M+1], x[2M+1]\ldots\}$ …

$$x(n) = \sum_{r=0}^{M-1} x_r(n)$$

The same is applicable to h(n)

$h_0(n) = \{h[0], h[M], h[2M]\ldots\}$

$h_1(n) = \{h[1], h[M+1], h[2M+1]\ldots\}$ …

$$h(n) = \sum_{r=0}^{M-1} h_r(n)$$

$$y(n) = \sum_{r=0}^{M-1} x_r(n) * \sum_{r=0}^{M-1} h_r(n)$$

If the filter has n-length, then the Z- transform of its transfer function is

$H(z) = h(0) + h(1)z^{-1} + h(2)z^{-2} + h(3)\, z^{-3} + \ldots + h(n)\, z^{-n}$

This can be rearranged in the polyphase realization form as shown in Fig 7; assuming M = 2

$H(z) = (h(0) + h(2)\, z^{-2} + h(4)\, z^{-4} + h(6)\, z^{-6} + \dots) + (h(1)\, z^{-1} + h(3)\, z^{-3} + h(5)\, z^{-5} + h(7)\, z^{-7} + \dots)$

$H(z) = E(z^2) + z^{-1}E(z^2)$

$H(z) = (h(0) + h(2)\, z^{-2} + h(4)\, z^{-4} + h(6)\, z^{-6} + \dots) + z^{-1}\,(h(1) + h(3)\, z^{-2} + h(5)\, z^{-4} + h(7)\, z^{-6} + \dots)$

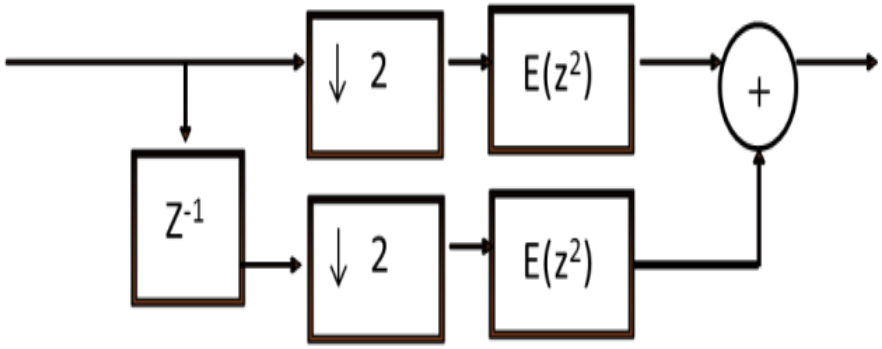

Fig 7: decimation by 2 polyphase decomposition

In MATLAB/Simulink implementation, the polyphase decimation concepts were used with pipeline frequency transform channelization algorithm and polyphase fast Fourier transform channelization algorithm within the inverse sinc lowpass filter and the final lowpass filter.

2.6 Computational Complexity Estimation

The computational complexity estimates of the three channelization algorithms are obtained by using the multiplications per input sample of operation of the system. This requires a correct estimation of the filter order or length. The filter order (N) for an FIR lowpass (Equiripple) digital filter is expressed using the developed optimized Kaiser's formula expressed as:

$$N = \frac{-20 * log_{10}\sqrt{\delta_p \delta_s} - 13}{14.6\,(w_s - w_p)/2\pi fs}$$

The peak passband ripple and stopband ripple are expressed as δ_p and δ_s with the passband edge w_p and stop band edge $w_s$normalized with the sampling.

The filter length therefore is expressed as the filter order plus one (N+1); this is used to express the computational burden or complexity of the system.

Multiplication per input sample = (N + 1) $* \frac{fs_{inp}}{M}$ in multiplications per second

3. RESULTS AND ANALYSIS

In order to obtain all these results certain settings are observed on the MATLAB/ Simulink environment:

a. First, a DSP Builder 12.1 was installed on MATLAB R2013a
b. In the Simulink environment, the data import/ export which was saved on the workspace must have a structure with time format

The output spectrum of the two filter configurations for per-channel algorithm is given in Fig 8.

Fig 8(a) shows that the digital filter signal passes 10.7 MHz intermediate frequency signal while other signals at fractions or harmonics of the individual intermediate frequencies at different sample rates are attenuated to a level approximately equal to -40 dBm; therefore, the difference between the noise floor and the signal strength at 10.7 MHz gives an SNR of 70 dBm.

Fig 8(b) shows that the spectrum from 10.7 MHz to 30.7 MHz which corresponds to 20 MHz FM spectrum passed through the filter. The spectrum shows signal attenuation equal to -40 dBm with an SNR of 70 dBm.

3.1 Per-Channel

This model gives output for 5 different channels with signal strength of about 120 dBm range on decimation by 128 within a frequency band of 100 kHz and when down sampled further by 2, the signal strength reduces to 100 dBm for a frequency range of 100 kHz as illustrated in Fig 9. This gives an estimate of the power consumption of the system. Since the CIC is common to the three algorithms, the computational complexity is estimated based on the inverse sinc final lowpass filter.

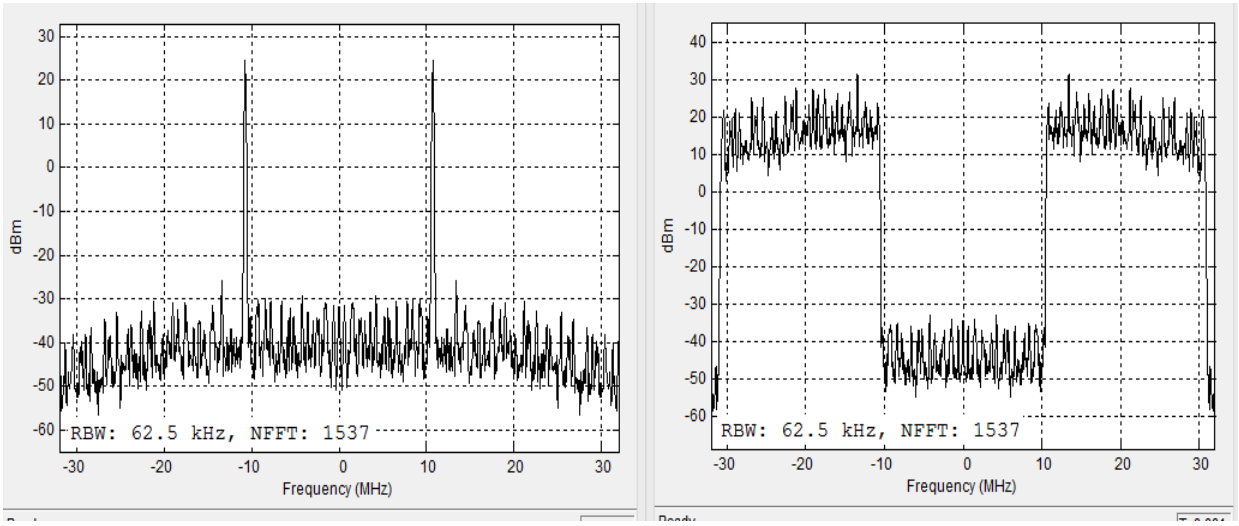

Fig 8: double sided spectrum of the two digital filter configurations for per-channel algorithm

The algorithm for the 5 different channels has the fastest compilation time compared to pipeline frequency transform and polyphase fast Fourier transform algorithm. A delay time of 3 seconds was observed before the start of the main compilation, then completely acquires the data needed within 12 to 19 seconds and ends the simulation at 36 seconds. The inverse sinc filter has a multiplication per input sample, addition per input sample, number of adders and multiplier of 29M multiplications/sec (mps), 28M multiplications/ sec (mps), 28, 29 respectively. This is because a down sampler is introduced after a single rate type minimum order filter. If the filter computation had undergone polyphase multi-stage decimation the multiplication per input sample would have been 7,250, 000 mps therefore saving about 21,750,000 mps and causing a reduction in computation of almost 4: 1.

3.2 Pipelined Frequency Transform (PFT)

The NCO configuration with the polyphase multi-stage decimation at the output stage, achieved a reduced computation algorithm for pipeline frequency transform channelization model. The outputs of each channel are as described in Fig 10, 11 and 12. The signal strength of about 100 dBm range was obtained for the decimation by 128 within a frequency band of 100 kHz on the first, fourth and fifth channel while for the second and third channel, the signal strength is about 80 dBm. Further down sampling by 2 reduces the signal strength of the first, fourth and fifth channel to approximately 80 dBm for a frequency range of 100 kHz while, the second and third channel has its signal strength reduced to approximately 60 dBm. Pipeline frequency transform for 5 different channels has the longest compilation time compared to per-channel and polyphase fast Fourier transform algorithm.

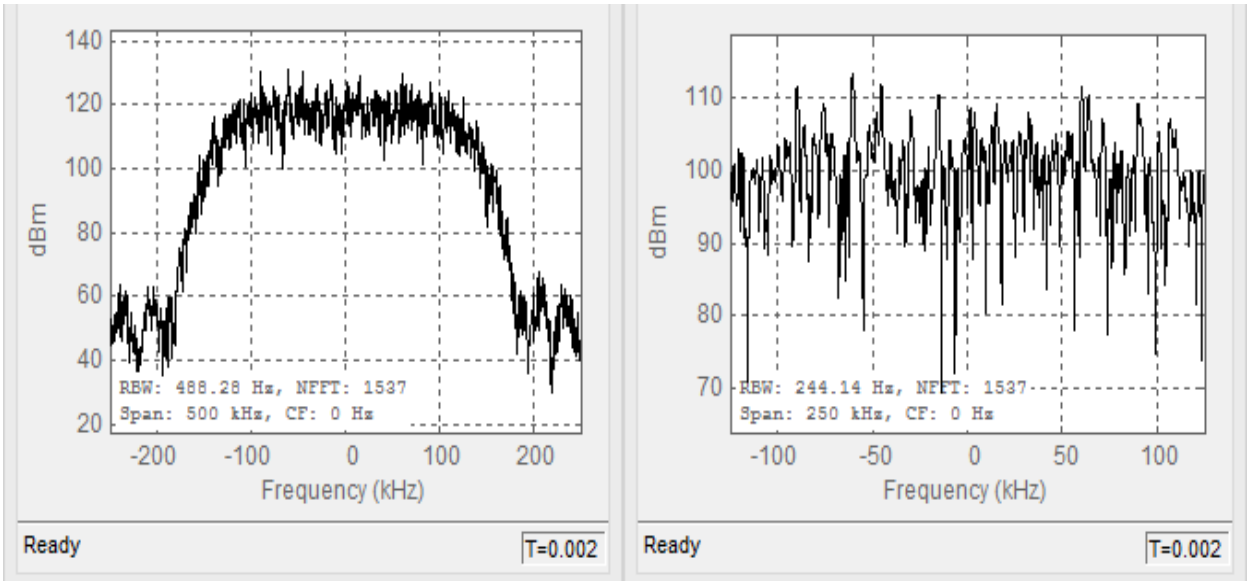

Fig 9: per-channel output after the decimation by 128 and 256

At the start of the simulation, a delay time of 10 seconds was observed before the start of the main compilation; this completely acquires the data needed after 6 minutes 43 seconds and finally ends the simulation at 7 minutes 10 seconds. The inverse sinc filter has a multiplication per input sample, addition per input sample, number of adders and

multiplier of 14.5M multiplications/sec (mps), 14M multiplications/sec (mps), 28, 29 respectively. The lowpass filter as well has a multiplication per input sample, addition per input sample, number of adders and multiplier of 7.5M multiplications sec (mps), 7M multiplications/sec (mps), 14, 15 respectively.

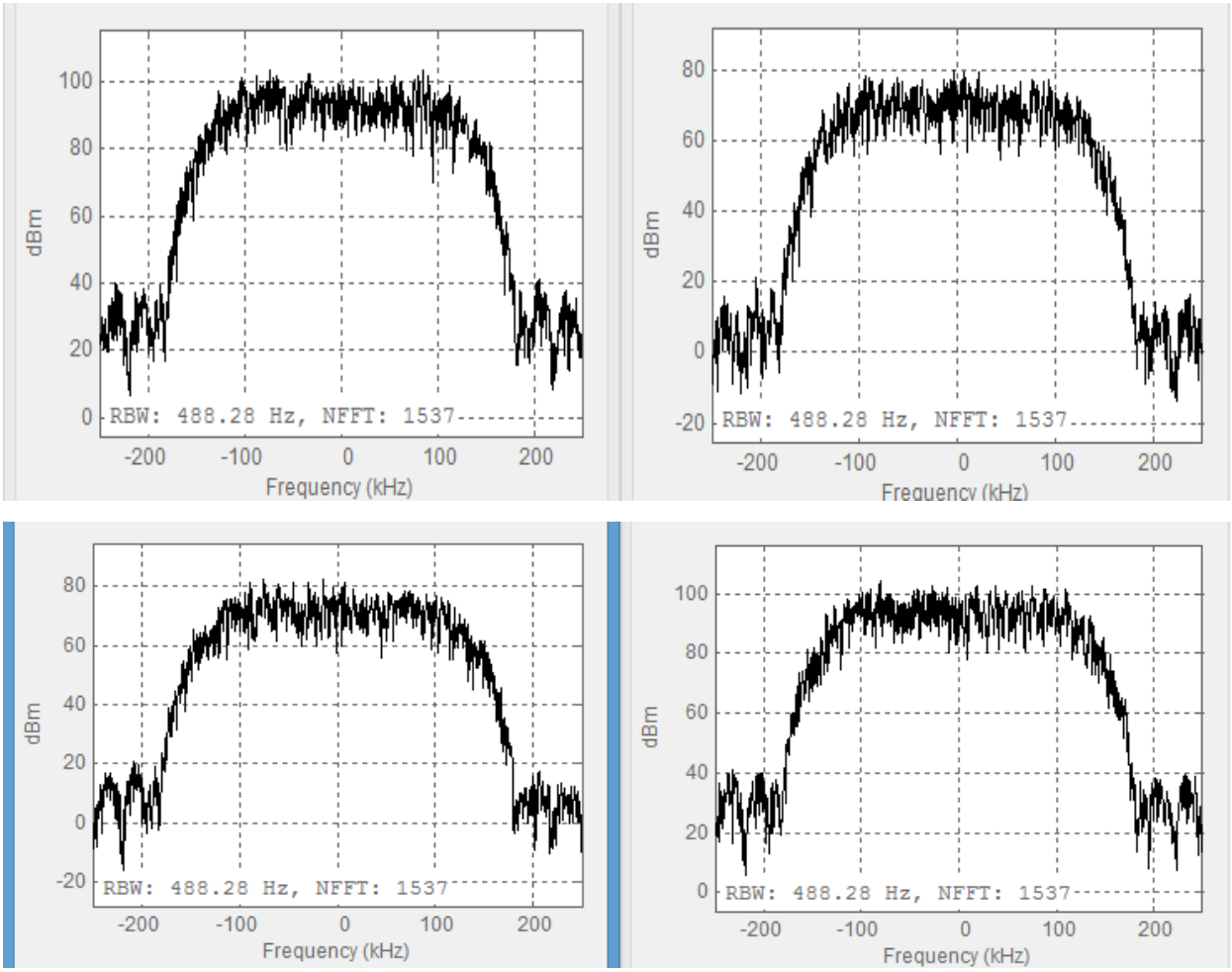

Fig 10: pipeline output after the decimation by 128 for channel 1- 4

3.3 Polyphase Fast Fourier Transform (Polyphase FFT)

The polyphase fast Fourier transform channelization algorithm has outputs of each channel as described in Fig 13. The signal strength of about 120 dBm range was observed for the decimation by 128 within a frequency band of 100 kHz and when down sampled further by 2, the signal strength reduces to 110 dBm for a frequency range of 100 kHz. The compilation time for the 5 different channels was observed to have a minimal time which falls between the time for per-channel channelization method and pipeline frequency transform method. A delay time of 16 seconds was observed before the start of the main compilation, then completely acquires the data needed within 24 to 34 seconds and ends the simulation at 51 seconds. PFT and PFFT at the rate conversion end, have the same inverse sinc and lowpass output estimation.

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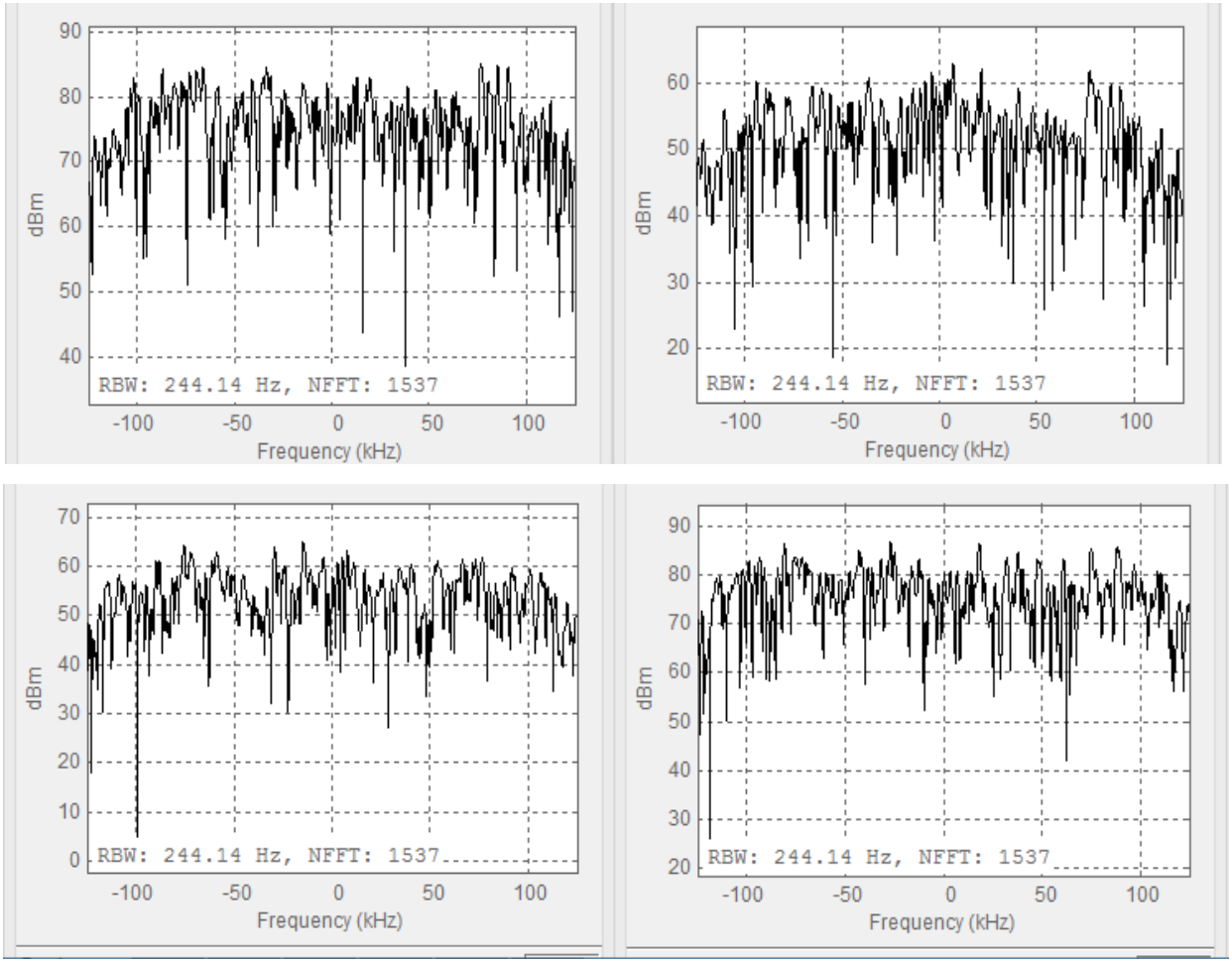

Fig 11: pipeline output after the decimation by 256 for channel 1- 4

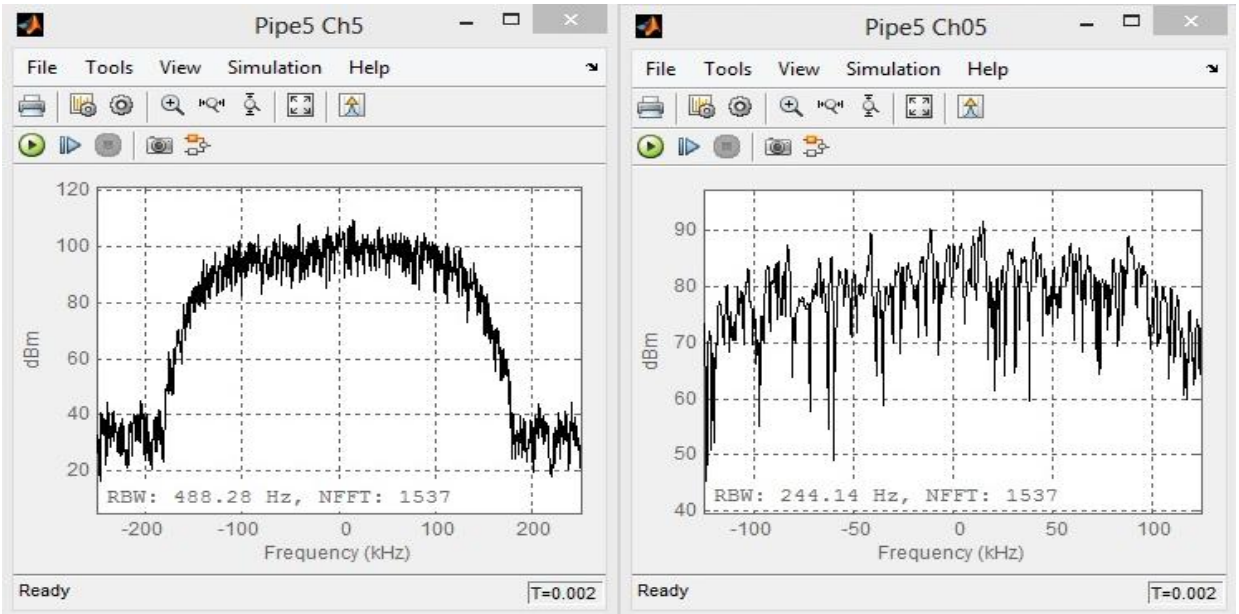

Fig 12: pipeline output after the decimation by 128 and 256 for channel 5

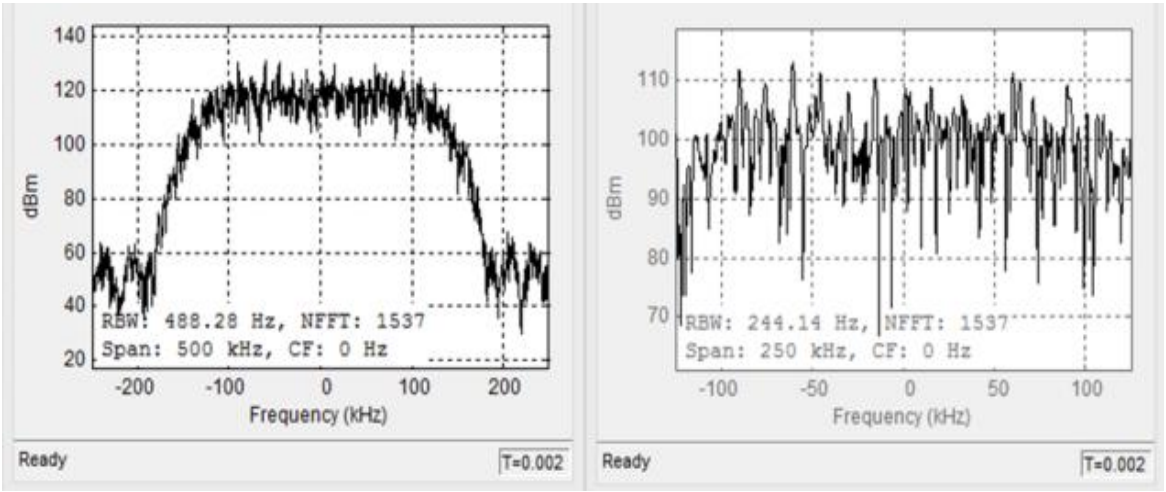

Fig 13: polyphase output after the decimation by 128 and 256

4. CONCLUSION

The total estimation of the computational burden for PFT and PFFT can be given as the sum of the individual multi stage. Therefore, the computational burden for the two stages is given as:

Overall multiplication per input sample = 14,500,000 + 7,500,000 = 22,000,000 multiplications/sec (mps).

This value shows a reduction of 7,000,000 multiplications per input sample which is equivalent to 24% decrease when compared to per-channel. In comparison, the PFT and PFFT having similar designs at the sample rate conversion end differ from each other in that the PFT divides the input spectrum into high pass and low pass frequencies and forms an hierarchical structure therefore increasing the silicon cost of PFT over PFFT.

The signal strength of each algorithm shows that the per-channel and PFFT have similar power spectrum characteristics and the resulting signal strength over a 250 kHz bandwidth varies about 100-110 dBm. Whereas, the signal strength for PFT varies between 40–90dBm characterized with numerous spikes between the 250 kHz bandwidth.

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