Low Complexity Farrow Differential Channelizer Algorithm

Temidayo Otunniyi
Federal Uni. of Tech., Akure
Computer Resource Center
Vice Chancellor's Office

Adedotun O.Owojori
Federal Uni. of Tech, Akure
Dept of Elect/Elect
School of Eng & Eng Technology

Erastus O. Ogunti
Federal Uni. of Tech., Akure
Dept of Elect/Elect
School of Eng & Eng Technology

Akinlolu A. Ponnle
Federal Uni. of Tech., Akure
Dept of Elect/Elect
School of Eng & Eng Technology

ABSTRACT

Reduction in hardware complexities is vital in communication. The major contribution to hardware complexity in many technologies is the multiplier utilized. This work present a proposed algorithm based on Farrow differential polynomial interpolation. This interpolator filter is a time varying poly-phase filter that uses fractional delay to reduce the integer sampling rates to fractional rates. It is a novel polynomial interpolator with less multiplier usage and inherent linear phase low pass filter. The digitized intermediate frequency (IF) by ADC is derived from mixing the signal RF with a local oscillator signal of a given fixed/variable frequency. Digitization using an analog to digital converter (ADC) capable of running at a sampling time of greater or twice the IF with maximum dynamic range of 100 MHz [This is contrary to the direct down conversion of multiband RF to band pass signals where under sampling is used. The algorithm was designed using Altera Digital Signal Processing tool box in MATLAB/ Simulink environment. When implemented it leads to reduction in the computational complexity, power consumption and silicon area. It also showed that a power gain of -15 dBm was observed as output for the GSM channel when compared with the existing modified farrow algorithms which have power gain of -9.4dBm and farrow polynomial algorithms with power gain of 10.59dBm. The decimation factor of 260 for a frequency range of 270.70 kHz was used. Thus a remarkable lower power gain, lower complexity and lower power consumption in mobile system was obtained when compared to farrow polynomial algorithm and modified farrow algorithm.

General Terms

Algorithms, Interpolator filter, Differential Polynomial

Keywords

Farrow Differential algorithm, Channelization, Multirate Digital Filter Bank, Software Defined Radio, Digital Down Conversion

1. INTRODUCTION

Reduction in hardware complexities is vital in communication. The major contribution to hardware complexity in many technologies is the multiplier utilized. The multipliers usually leads to remarkable increase in the silicon area (as in the case of FPGA), increases the power consumption, and lowers the speed of the system. Most communication systems are mobile systems and as such require portability, low power consumption and speed to meet the needs and the satisfaction of the end users. In an attempt to meet the specifications of mobile systems, there is the need to reduce the complexity of the hardware mostly in terms of silicon area and power consumption. This goal can be achieved by replacing the overall multipliers used with low cost, low power components such as adder and shift registers.
Software Defined Radio (SDR) provides means of realizing as many signal processing task as possible in the trans-receiver communication module by means of software. These modules are usually driven by digital signal processors together with accelerators such that the digital signal processors appear to be the computing engine.

Different communication standards require different master clock and in order to ensure quality clock rates, digitized sample rate converters are used. This is to convert from one sample rates to another (usually from higher to lower) while preserving the necessary information in certain frequency band. However different rate changes, stop-band and pass-band attenuation varies and this affects the reconfiguration of the Software Defined Radio. Sample rate conversion (SRC) takes place at each ADC or DAC interfaces. Depending on the functionalities and the information to be preserved, different SRC solutions exists, among which are interpolators, decimators, etc.

Different algorithms have been proposed for reducing hardware complexities. The Integer SRC with poly-phase decimator or poly-phase interpolator has been found to be efficient for low complexity filter length but with high interpolator rate. Farrow interpolation filter, Modified Farrow filter, and Taylor series approximation proved to have the ability to reduce the complexity for either the integer or fractional SRC. It was shown **[1]** that a low complexity interpolator can be designed using Farrow structure **[2, 6, 7, 8]**. The coefficients of Farrow Structure are fixed for a given order N and there is no need for updating the sub-filter co-efficient. The co-efficient of Farrow Structure determines the power consumption in dBm. Transposed Modified Farrow Structure **[11, 12]** has lower sample rate and low computational complexity. Modified Farrow structure **[3]** has been proven to be efficient for implementing rational sampling rate conversion **[4], [3]** by reducing the number of operator in Farrow structure. The complexity reduction can be achieved by changing the range of the delay parameter so that the integer part of the coefficient is removed.

This paper focuses on developing a novel farrow interpolating algorithm. Farrow differentiation interpolation polynomial is an approximation technique that yields exact values instead of round off values. The differentiation of the farrow filter leads to reduction in the coefficients generated and the number of multipliers and this leads to reduction in the complexity of hardware in digital systems in terms of silicon cost, area of hardware resources as in the case of FPGA, clock speed and power consumption.

2. RESEARCH METHOD

2.1The whole system is analogous to that of super heterodyne receiver architecture as shown in Figure 1.

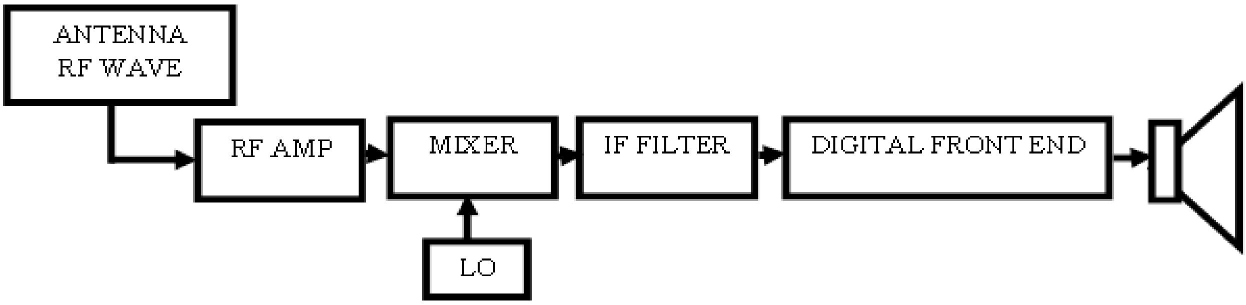

Fig 1: The block diagram of the super- heterodyne radio receiver

Based on this architecture, the RF analogue signal was modelled base on available real GSM channels by the use of MATLAB/Simulink software. This RF signal enters the receiver through the antenna which is either incorporated into the FPGA board or designed on an expandable circuit before incorporation into the FPGA board. Instead of dealing with high dynamic ranges or requirements and sampling frequency required for the simulation of the RF signals based on Nyquist criterion in the radio frequency section of the radio receiver, the intermediate frequency (IF) was used, which was derived from mixing the signal RF with a local oscillator signal of a given fixed or variable frequency. The IF obtained allows easy digitization of the signals by using an analogue to digital converter (ADC) capable of running at a sampling time of greater or twice the IF with maximum dynamic range of 100 MHz **[9]**. This is contrary to the direct down conversion of multiband RF to band pass signals as described by **[9]** where under sampling was used. The Global System for Mobile Communication (GSM) system is a Frequency Division Multiplexing Access / Time Division Multiplexing Access (FDMA/ TDMA) system. Each physical channel is characterized by a carrier frequency and a time slot number. GSM system frequencies include two bands at 900 MHz and 1800 MHz commonly referred to as GSM-900 and DCS-1800 [13]. For the primary band in GSM-900 system, 124 radio carriers have been defined and assigned in two sub-bands of 25 MHz each in the 890-915 MHz and 935-960 MHz ranges, with channel width of 200 KHz. The stream of sampled speech data is fed into a source encoder in which case Bernoulli random number was used to compresses the data by removing unnecessary redundancy. The Bernoulli random number is probabilistic in nature with the probability equal to ½ and the M-nary bits generated set to 4. The sample time used is twice the maximum sampling frequency, f_m, 960 MHz, thus the sample time used is 1/2 × f_m.

The analog front end starts using the Bernoulli binary generator where the bits are generated randomly with M = 2^b= 2^{2m}= L^2 –ary

Where b is the no of bits per symbol; L is the modulating order and m is the message per frame.

Assuming the number of sample times = N_s= b × N_b

The number of samples per second, N_{bsps} = b ∗ 2^3

$$\text{b} = \frac{R_B}{Channel\ Bandwidth}$$

$$\text{B}T_b = \frac{1}{Channelbandwidth} = \frac{1}{R_b}$$

w_c = $2\pi f_c$

Binary Convolutional Encoder with K (=2) - bits input and N (=3) - bits output and L -1 (=3) 2 bits registers having $2^{(L-1)K}$ = $2^{3.2}$=64 states.

Code rate = $\frac{K}{N}$

$$s_m(t) = A_{mc}S_{uc}(t)\ + A_{ms}S_{us}(t)$$

$$\text{Re}\left\{(A_{mc}\ +\ jA_{ms})\sqrt{\frac{2}{T_s}e^{j\omega_c t}}\right\}$$

For m = 1, 2… M-1

$$A_{mc}\sqrt{\frac{2}{T_s}}\ \cos(\omega_c t)\ - A_{ms}\sqrt{\frac{2}{T_s}}\ \sin(\omega_c t)$$

$$= A_m\sqrt{\frac{2}{T_s}}\ \cos(\omega_c t\ \ +\theta_m)\ ;$$

$$= A_m = \sqrt{A_{mc}{}^2 + A_{ms}{}^2}$$

For 0 ≤ t ≤ T_s

$$\theta_m = \tan^{-1}\frac{A_{ms}}{A_{mc}}$$

$$S_{uc}(t) = \sqrt{\frac{2}{T_s}}\ \cos(\omega_c t)\ ;\ S_{us}(t) = \sqrt{\frac{2}{T_s}}\ \sin(\omega_c t)$$

H =1/2 (modulating index)

T= bit duration

$$\mathrm{x(t)} = \cos(2\pi f_c t + \emptyset(t))$$

$$\emptyset(t) = 2\pi \mathrm{h} \int_{-\infty}^{t} \sum_{-\infty}^{+\infty} a_k \left((s(\tau - KT\right)\delta(t)$$

where a_k = binary data in bits (+/- 1)

The analog RF signal is converted to IF signal, which involves the multiplication of the incoming RF signal with a reference local oscillator signal. One of the major purposes of the SDR is to replace all analog components with digital components. To do so, the low pass filter required at the IF end is preferably a digital low pass filter which must convolve with a discrete IF signal. Besides, all channelization tasks are performed digitally; in other words, there must be a signal conversion from analog to digital which requires a rate converter from the initial sampling rate of 2.5 GHz to 160 MHz. The digitized intermediate frequency (IF) by ADC is derived from mixing the signal RF with a local oscillator signal of a given fixed/variable frequency. Digitization using an analog to digital converter (ADC) capable of running at a sampling time of greater or twice the IF with maximum dynamic range of 100 MHz **[10]**. This is contrary to the direct down conversion of multiband RF to band pass signals as **[10]** where under sampling is used.

The digital front end starts from the generation of digital signal by the ADC to the channelization stage in the system design. The output of the ADC can be expressed below as a sum of weighted impulses. Assuming Y_a[n] = x[n]:

$$x[n] = \sum_{k=-\infty}^{\infty} x(k)\delta(n) - (k)$$

where the response of the system to x[n] is the corresponding sum of weighted outputs y(n), therefore:

$$\mathrm{y(n)} = \tau(\mathrm{x[n]}) = \tau\left[\sum_{k=-\infty}^{\infty} \mathrm{x(k)}\ \delta(\mathrm{n-k})\right]$$

$$= \sum_{k=-\infty}^{\infty} \mathrm{x(k)}\ \tau[\ \delta(\mathrm{n-k})]$$

$$= \sum_{k=-\infty}^{\infty} \mathrm{x(k)\ h(n-k)}$$

$$\sum_{k=0}^{M} \mathrm{x(k)\ h(n-k)} = \sum_{k=0}^{M} \mathrm{h(k)\ x(n-k)}$$

The digital down converter (DDC) is an important component in any digital radio since it performs frequency translation from 69.9 MHz to baseband at a high input sample rates as that of the analog to digital converter (ADC). The convolved output of the input digital signal and the digital filter enters an input on the mixer which mixes with a numerical controlled oscillator (NCO) signal having a frequency f_{LO} of 69.9 MHz and sampling rate of 160 MHz to generate a sine, cosine or complex wave

The NCO is capable of generating a multichannel real or complex sinusoidal signal depending on a real input IF signal. These NCO signals have independent frequency and phase in each output channel with amplitude of the created signal equal to 1.

To generate a given desired output frequency F_0, the value of the phase increment within the phase accumulator must be determined. Phase increment = ($\frac{F_o\,.2^N}{F_s}$). The frequency resolution of an NCO is defined by $\Delta f_r = \frac{1}{T_s.2^N}$

Given a desired phase offset (in radians), the Phase offset block parameter was calculated with

$$\text{Phase offset } = \frac{2^N.\,desired\ phase\ offset}{2\pi}$$

The spurious free dynamic range (SFDR) is estimated as follows for a lookup table with 2^{P} entries,

SFDR = (6P) dB without dither and SFDR = (6P + 12) dB with dither. Where P is the number of quantized accumulator bits and N is the accumulator word length. The block uses a quarter wave lookup table techniques that stores table values from 0 to pi/2. The block calculates other values on demand using the accumulator data type and cast them into the output data type.

2.2 FRACTIONAL SAMPLE RATE CONVERTER

In digital signal processing, Interpolation means up-sampling together with anti-imaging filters. The anti-image filter actually does interpolation in the real sense. The fractional decimation is incorporated as anti-aliasing filter. The intermediate sample time is the ratio of the input rate and the output rates. Output rate determined the inter-sample time. However in certain application which involves the fractional sample rate, the fractional sample rate is determined from the ratio of two positive integers $\left({}^{L}\!/_{M}\right)$ fractional.

The input parameters n1 and μ1 are used to determine the time instant t_1 for the l th new output sample $y(l)$=$y_a(t)$ as t_1 =$(n_1 + \mu_1)T_{in}$.

Given t_1, the parameters

$$n_1 = \left\lfloor {}^{t_1}\!/_{T_1} \right\rfloor \text{ and}$$

$$\mu_1 = {}^{t_1}\!/_{T_1} - \left\lfloor {}^{t_1}\!/_{T_1} \right\rfloor$$

The convolution

$$y(l) = \sum_{K=-N/2}^{\frac{N}{2}-1} x(n_1 - k)\, h(k, \mu_1)$$

Where N is the filter length and $h(k, \mu_1)$ is the impulse response of the interpolation filter.

The fractional Interval μ_1 determines the coefficient values of the impulse response $h(k, \mu_1)$

And its value is in the interval of {0, 1}. In order to find the new output sample values $y(l)$, we propose Farrow Differentiating Interpolation filter structure as shown in Fig 2. Implementing the impulse response using CIC is feasible for integer sample rate conversion resulting in low complexity, but for arbitrary sample rate, the realization is difficult to implement because part of the filter have to be clocked at the high intermediate sample rate which further limit the applications to small values of L and M.

The way out of implementing fractional sample rate conversion is to use the time varying poly-phase structure. This requires cascading the poly-phase interpolator and up-sampler and farrow filter or with poly-phase decimator and down-sampler.

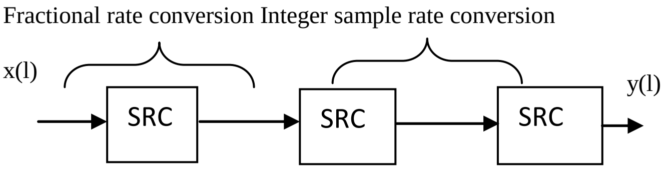

Fig 2: Cascade of fractional sample rate conversion

Proposed Farrow Differentiating Interpolating Filter STRUCTURE

Farrow differentiating Interpolation filter provides another approach for implementing fractional delay filters using LaGrange polynomials. It uses piecewise approximation of the filter into a polynomial that shares a common set of coefficients. This result in interpolation of input signals. Two important design parameters are polynomial order (L) and Farrow sub-filter Length (N). Farrow differentiation filter is implemented as a direct form of FIR filter structure. It is obtained as approximation of continuous time function $X_c(t)$ by fractional delay D.

$$y(n) = h(d) * x(n) \qquad (1)$$

$$y(n) = h(n,d) * x(n) = X(n-D) = \sum C_K D^K \qquad (2)$$

The coefficients C_K are solved from the set of N + 1 Linear equation. This coefficients are expressed in terms of the fractional delays such that $0 \le d \le 1$.

$h(n)$ can be expressed as $C_0 + C_1 + C_2 + - - - - + C_n$
Differentiating x(n)

$$D^V x(n) = \lim_{t\to 0} \sum_{k=0}^{\infty} C_K \; x(n-kt) \qquad (3)$$

Truncating $D^V y(n)$

$$D^V x(n) \approx \lim_{t\to 0} \sum_{k=0}^{\infty} C_K \; x(n-kt) \qquad (4)$$

Removing the limit,

$$D^V x(n) \approx \sum_{k=0}^{\infty} C_K x(n) \qquad (5)$$

Let $n = (n-D)$

$$D^V x(n-D) = \sum_{K=0}^{k} C_K \, x(n-D)$$

But $x(n-D)$ *are non integers delay sample of signal* $x(n)$

$$x(n-D) = \sum_{r=0}^{N-i} d^k \, x(n-D)$$

$$D^V x(n-D) = \sum_{K=0}^{P} C_K \sum_{r=0}^{N-i} d^k \, x(n-D)$$

$$= \sum_{r=0}^{N-i} \left[\sum_{K=0}^{P} C_K \; d^k \right] x(n-D)$$

Let

$$h(d)' = \sum_{K=0}^{P} C_K \; d^k \qquad (6)$$

$$D^V x(n-D) = h'(d) * \mathrm{x}'(\mathrm{n})$$

The structure can be expressed in z domain as

$$H'_d\,(Z) = \sum_{n=0}^{N} h^{'(n,d)} \, Z^{=n}$$

$$= \sum_{n=0}^{N} \left| \sum_{k=0}^{p} C_k{}'(n) d^k \right| z^{-n} \qquad (7)$$

Where $h'(n,d)$=
$C_0 + C_1 d^1 + C_2 d^2 + - - - - + C_n d^n = \left| \sum_{k=0}^{p} C_k{}'(n) d^k \right|$

The determinant of the equation above is called Vander mode determinant formed from $d_0 , - - d_n$

$$\mathrm{H}\,(d_0 , - - d_n) = \begin{vmatrix} 1 & d_0 & d_0^2 & d_0^n \\ 1 & d_1 & d_1^2 & d_0^n \\ 1 & d_n^1 & d_n^2 & d_n^n \end{vmatrix} \qquad (8)$$

$$\mathrm{h'}(d_0 , - - d_n) = C_k{}'(d - d_0)\,(d - d_1)\,(d - d_1)\ldots\ldots (d - d_{n-1}) \qquad (9)$$

$$\mathrm{h'}(d_0 , - - d_n) = \prod_{i>i}^{n} \; (d_i - d_j) \qquad (10)$$

$C_k{}'$ depends on the value of $d_0 , - - d_n$

Let

$$C_{k'}(n) = L_K(d) \qquad (11)$$

This equation above can be rewritten as

$$\mathrm{h}(d_0 , - - d_n) = L_0(d)h(d_0) + L_1(d)h(d_1) + \ldots\ldots\ldots\ldots\ldots\ldots + L_n(d)f(d_n) = \sum_{k=o}^{n} L_K(\mathrm{d})\mathrm{h}(d_k) \qquad (12)$$

$$H_d\;'(Z) = \sum_{n=0}^{N} h'(n,d)\, Z^{=n} \qquad (13)$$

The conceptual view of the farrow Differential algorithm is shown in Fig 3.

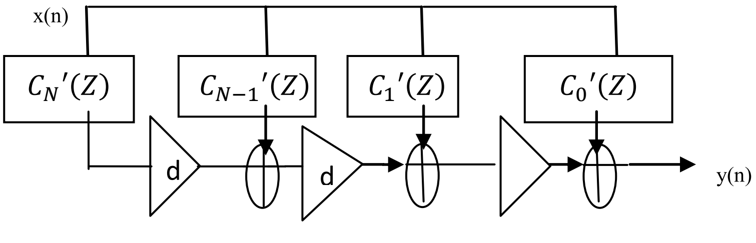

Fig 3: Conceptual view of farrow Differential algorithm

The digitized rate as shown in fig 5 is set to 160 MHz, and the GSM sample rate is 69.93 MHz In order to convert the sample rate from 160 MHz to fractional sample rate of 69.93 MHz, the fractional rate conversion of 13/30 is required. Farrow differential algorithm is used to replace the normal conventional FIR filter. The digitized rare of 160 MHz is up-sampled by 13, followed by farrow differential interpolator filter and then decimated by down-sample of factor 30 with the fractional delay μ set to 13/30= 0.499. This set the new output sample rate at 69.93MHz. In order to take the signal to baseband, the new sample rate is decimated further by integer factor of 260 to get the output rate of 270 kHz.

3. RESULTS AND ANALYSIS

In order to obtain all these results certain settings are observed on the MATLAB/ Simulink environment:

a. First, a DSP Builder 12.1 must be installed on MATLAB R2013a

b. In the Simulink environment, the data import/ export which will be saved on the workspace must have a structure with time format

Fig: 4 shows the result of farrow differential algorithm. The power gain of -15dBm was observed as output of farrow Differential algorithm. The decimation factor of 260 was used to baseband the GSM to frequency of 270.70 kHz. Thus a remarkable lower power gain, lower complexity and lower power consumption were observed when farrow differential polynomial algorithm was used compared to farrow polynomial algorithm and modified farrow algorithm. This is as a result of adder and shift registers used during the design of Farrow Differential Algorithm and also the silicon area was reduced.

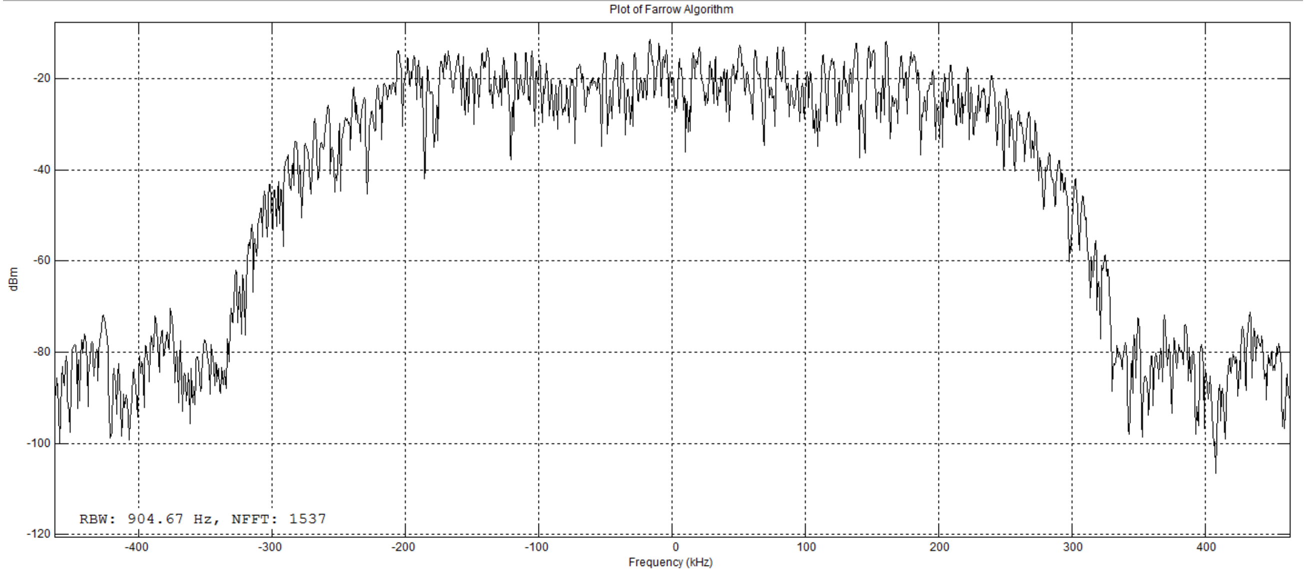

Fig 4: Result of decimation the fractional sample rates by 260

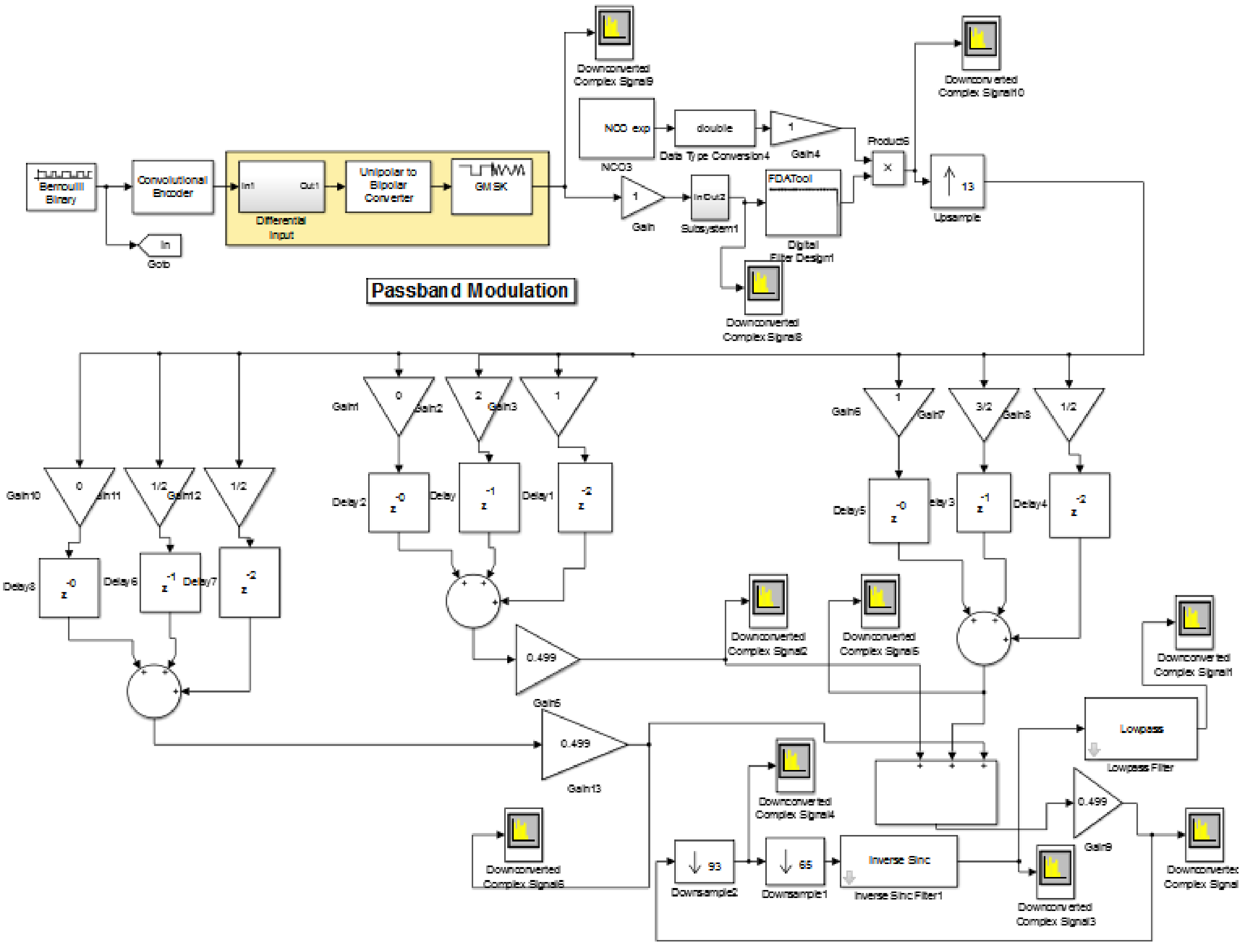

Fig 5: The farrow Differential Algorithm

4.CONCLUSION

The filter length of conventional filter order is very long and this constitutes remarkably to the complexities of the hardware. In order to minimize the filter order, a method is devised to this effect using Farrow differentiation polynomial interpolation. This fractional sample rate conversion requires exact filter with little or no error. This sampling rate conversion method yields output signal that is $^{L}/_{M}$ times the original input sample rate.

Farrow differentiation interpolation polynomial is an approximation technique that yields exact values instead of round off values. The differentiation of the farrow filter leads to reduction in the coefficients generated and the number of multipliers and this leads to reduction in the complexity of hardware in digital systems. The algorithm also results in lower power gain of -15dBm compared to the existing farrow algorithms with power gain of 10.59dBm and modified farrow algorithm with power gain of -9.4dBm. thereby yielding reduction in terms of silicon cost, area of hardware resources as in the case of FPGA, clock speed and power consumption.

5. REFERENCES

[1] Rouphael, T.J. (2009). RF and Digital Signal Processing for software Defined Radio. Pp 371-375. Elsevier Inc.

[2] Farrow, C.W. (1988), A Continously Variable Digital Delay Element. 2641-2645. IEEE International Symposium.

[3] Laasko, T., Valimaki, V., Karjalainen, M. and Laine, U. (1996). Splitting the Unit Delay. IEEE Signal Processing Magazine. Vol. 13. Pp: 30-60.

[4] Valimaki,V, A new filter implementation strategy for Lagrange interpolation,"*Proc. IEEE Int. Symp. Circuits and Systems*, pp. 361–364,

[5] Hermanowicz, E. (2004), On designing a wideband fractional delay filter using the Farrow approach," in Proc. EUSIPCO'2004, Austria, Sep. 6–10, pp. 961–964.

[6] Farrow,C.W .(1988), A continuously variable digital delay element," in Proc. IEEE ISCAS'88, Espoo, Finland, 1988, pp. 2641–2645.

[7] Blok, M. (2005), Farrow structure implementation of fractional delay filter optimal in Chebyshev Sense, in Proc. SPIE, vol. 6159, Wilga, Poland, p. 61594.

[8] Harris, F. J.(1997) , Performance and design of Farrow filter used for arbitrary resampling, in Proc. *DSP'97*, vol. 2, Santorini, Greece, 1997, pp. 595– 599.

[9] Hentschel, T., Henker M., and Fettweis G. (1999), The Digital Front- End of Software Radio Terminals, *IEEE Personal Communications*, pp 6-12.

[10] Ching-Hsiang, T. and Sun-Chung, C. (2006), Direct Down Conversion of Multiband RF Signals using Band Pass

[11] Johansson, .H and Lowenborg, P. (2003), On the design of adjustable fractional delay fir filters. Circuits and Systems II: Analog and Digital Signal Processing, *IEEE Transactions* on, 50(4):164– 169.

[12] H°akan Johansson. (2011), Farrow-structure-based reconfigurable bandpass linear-phase fir filters for integer sampling rate conversion. Circuits and Systems II: Express Briefs, IEEE Transactions on, 58(1):46–50

[13] Eberspacher,J.,Vogel, H.,, Bettstette, C. and Hartman,C. (2009) "GSM-Architecture, Protocols,Services". 3rd Edition. John Willey and Sons. Germany.