Communications on Applied Electronics (CAE) – ISSN : 2394-4714
Foundation of Computer Science FCS, New York, USA
Volume 2 – No.3, June 2015 – www.caeaccess.org

Design of BPSK/QPSK Modulator using Verilog HDL and Matlab

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ABSTRACT
Quadrature Phase Shift Keying (QPSK) is a modulation scheme commonly used in wireless communication system and it's because of its ability to transmit twice the data rate for a given bandwidth. In most cases, the QPSK modulator consumes less power and bandwidth in a modern devices but for a system like satellite and mobile devices where their operations are power limited, this is a problem that needs to be fixed. The objective is to design the QPSK modulator that uses less power for operation and it should be bandwidth efficient. The proposed technique uses data stored inside a memory block to produce a symbol according to the given input data. The QPSK modulation process requires a Direct Digital Synthesizer (DDS) to produce sine and cosine wave which are used as carrier signal with the data signal to produce QPSK/BPSK output signal. The proposed modulator successfully modeled with Verilog Hardware Description Language (HDL), simulated with Xilinx Integrated Software Environment (ISE) version 14.5 software. QPSK modulation is also performed on MATLAB tool, which gives three types of waveforms. 1) In-phase component, 2) Quadrature phase, and 3) Composite of both. After that the QPSK demodulator has been developed using MATLAB tool in order to verify the functionality of the modulator.

Keywords
Binary Phase Shift Keying, Quadrature Phase Shift Keying, Direct Digital Synthesizer, Bit Error Rate, Signal to Noise Ratio

1. INTRODUCTION
Modulation is the process of combining data signal and carrier signal. There are two types of modulation techniques i.e., Analog and Digital. In the analog modulation technique carrier signal is being modulated with the help of the analog data signal such as AM, FM, and PM. In digital modulation technique carrier signal is being modulated with the help of digital data signal. They are known as keying techniques e.g. ASK, FSK, PSK. The change in phase of carrier signal is called phase shift keying like BPSK, QPSK, 8-PSK, 16-PSK etc. In QPSK, two signals can be modulated at the same time. Its BER (Bit Error Rate) is lower than higher order PSKs such as 8-PSK, 16-PSK, etc. and they also easily get affected through noise. Higher order PSKs always consume more power and have complex circuitry when we compare it to the QPSK. BPSK/QPSK has moderate data transfer speed practically, more bandwidth efficient as well as power efficient [3]. When we compare the QPSK and BPSK, The main advantage of BPSK is that it requires the lowest C/N ratio. While, the drawback is that, the data rate achieved using BPSK is very low. QPSK is basically two BPSK links with their carriers in phase quadrature and operating on the same radio channel. Therefore the BER of both QPSK and BPSK remains the same. At the same time data rate gets doubled. MSK also considered as one type of PSK technique and for this we require complex circuit and higher bandwidth than QPSK. This project demands higher data rate without more use of bandwidth and power. Because of these trade-offs, we decided on using QPSK modulation scheme. In QPSK quadrature means four different states which are used to represent a group of 2 bits of input data and the four different inputs are 00, 01, 10 and 11 and from this each group takes one form of QPSK states as shown in table 1 [1].

Table-1 QPSK phase with different input symbol

Input	QPSK Phase
00	135°
01	225°
10	45°
11	315°

The other modulation scheme that is closely related to QPSK is BPSK (Binary Phase Sift Keying). If we think practically then, QPSK is formed from 2 separate BPSK which is combined together to form one QPSK. Therefore, the data transmission rate in QPSK is twice as compared to BPSK and the Bit Error Rate (BER) over signal to noise ratio (SNR) for both QPSK/BPSK modulation schemes are same [8]. QPSK symbol period is 2 times of the bit period, Ts=2Tb. In case of BPSK the symbol period is same as bit period Ts=Tb [1].

2. CONVENTIONAL MODULATOR
QPSK (Quadrature Phase Shift Keying) is one of the modulation schemes used in wireless communication system due to its ability to transmit twice the data rate for a given bandwidth. From the mathematical analysis, we can conclude that QPSK can be used either to double the data rate compared to BPSK. While maintaining same bandwidth of the signal, or to maintain the same data rate of BPSK but halving the bandwidth that is required [2]. The bit stream that coming in at a bit rate of Rb is taken by serial to parallel converter and splits it into two different streams i.e. I and Q, each of half the bit rate. These data-bits coming in as I (In-phase) and Q (Quadrature-phase) amplitudes are given to

the RRC filter. It will remove the all interference within the data bits and will forward that data bits to get combine with the sine and cosine signal, which is produced by the direct digital synthesizer. Both of these are then modulated individually by a sine or a cosine wave of carrier frequency ω after passing it from the root raised cosine filter. Both these I and Q signals are then added together to get the QPSK transmitted signal [5].

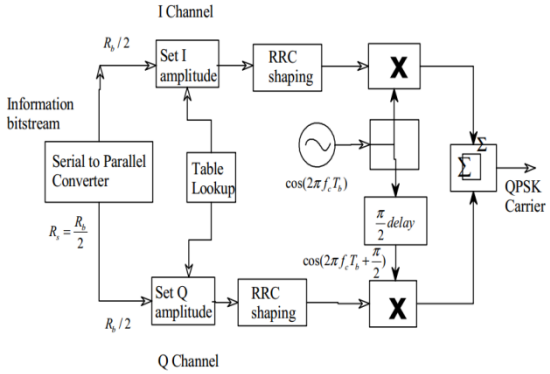

Figure-1 General block diagram of QPSK modulator [8]

SQPSK= $\sqrt{2Es/Ts}\ \cos(2\pi fct + (i-1)\frac{\pi}{2})$ for i = 1, 2, 3, 4. Where, $\sqrt{2Es/Ts}$ = Constant amplitude with Es energy and Ts = Time period of the signal, fc = Frequency of carrier signal, i = Phase no. of signal as per the symbols of the data signal from the trigonometric equation given below,

$\cos(a+b) = \cos a \cos b - \sin a \sin b$ [10]

3. QPSK CARRIER GENERATION USING MATLAB

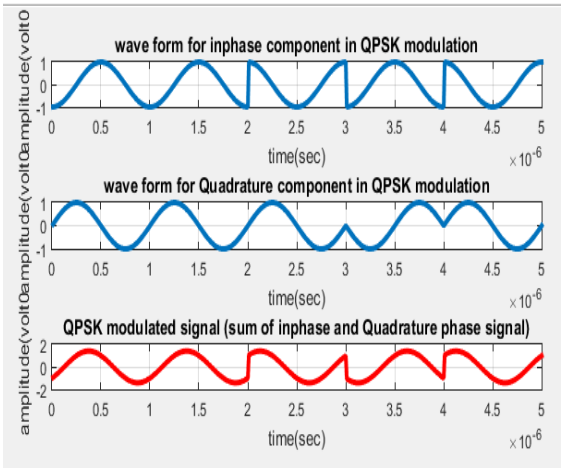

Figure-2 QPSK carrier generation

Here, if we want to generate QPSK carrier signal as shown in above figure. Then we just need to give the input bit stream of data at the input of the QPSK modulator. These bits are then divided into odd and even sequences by the serial to parallel converter. To remove the other interferences that may be exist in the data signal, both sequences must pass through the pair of RRC filter. Then this filtered signal will be combined with cosine and sine signal and ultimately we will get the QPSK carrier signal by combining both these signals.

4. BPSK & QPSK CONSTELLATION DIAGRAM

A constellation is a plot of I channel amplitude against the Q channel amplitude when sampled at the symbol rate. If the symbol rate is 5 seconds then, we would sample the time-domain signal every 5 second at the best possible moment and then plot the measured I and Q values. The figure 3 shows the QPSK constellation diagram. It is created by plotting the values of I and Q amplitudes. Each point is a pair of (I, Q) values representing a modulated signal or symbol. These In-phase and Quadrature-phase values are computed by multiplying the signal expression or its amplitude by sine or cosine of the phase angle [5].

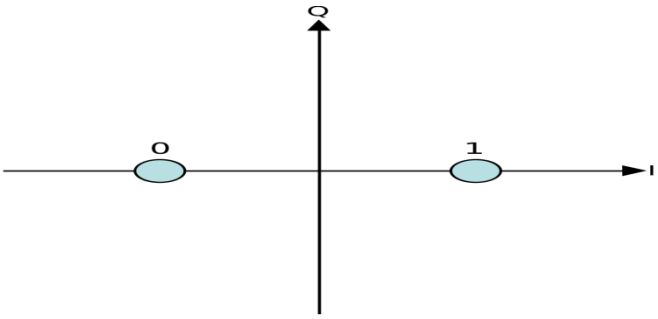

Figure-3 BPSK Constellation diagram

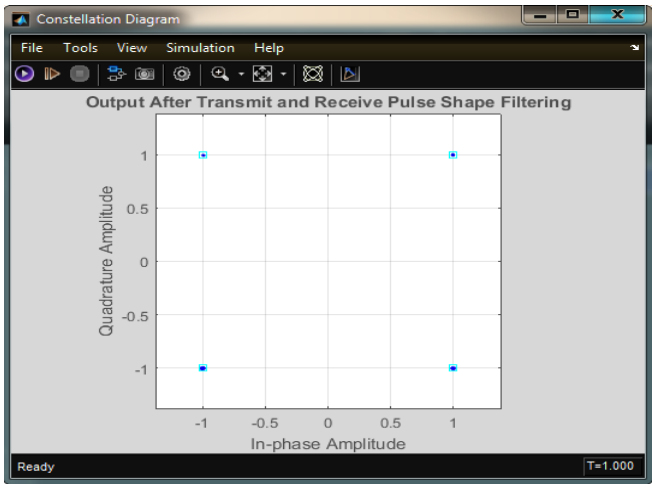

Figure-4 QPSK Constellation diagram

QPSK uses two basis functions, a sine and a cosine whereas BPSK uses only one. By varying the phase of each of these carriers, we can send two bits per each signal. The dimensionality of a modulation is defined by the number of basis functions used. This makes QPSK a two dimensional signal and it doesn't because it sends two bits per symbol, but because it uses two independent signals (sine and cosine) to create the symbols. As BPSK uses only one function, by combining two BPSK signals we can get the one QPSK signal.

Table-2 Phase shifted signal for different input symbols (BPSK) [5]

Symbol	Bit	Expression	Carrier Signal	I	Q
S1	0	$\sqrt{\frac{2E_s}{T}}\cos(\omega t)$		1	0
S2	1	$\sqrt{\frac{2E_s}{T}}\cos(\omega t + \pi)$		-1	0

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Table-3 Phase shifted signals for different input symbols (QPSK) [3]

Symbol	Bits	Expression	Phase, (Deg.)	Carrier Signal	I	Q
S1	00	$\sqrt{\frac{2E_s}{T}}\cos(\omega t+\pi/4)$	45		$\frac{1}{\sqrt{2}}$	$\frac{1}{\sqrt{2}}$
S2	01	$\sqrt{\frac{2E_s}{T}}\sin(\omega t+3\pi/4)$	135		$-\frac{1}{\sqrt{2}}$	$\frac{1}{\sqrt{2}}$
S3	11	$\sqrt{\frac{2E_s}{T}}\cos(\omega t+3\pi/4)$	225		$-\frac{1}{\sqrt{2}}$	$-\frac{1}{\sqrt{2}}$
S4	10	$\sqrt{\frac{2E_s}{T}}\sin(\omega t+\pi/4)$	310		$\frac{1}{\sqrt{2}}$	$-\frac{1}{\sqrt{2}}$

5. BPSK/QPSK MODULATOR BLOCKS

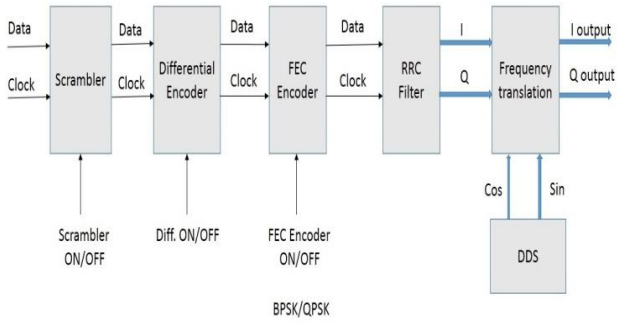

Figure-4 Top level block diagram of QPSK modulator [4]

The input data to the scrambler comes from external device which scrambles the data as per the CCITT V.35 standard. This scrambled data will be encoded differentially by differential encoder and then followed by FEC encoder. There is also mechanism available for the selection of the different blocks according to requirement. ON/OFF control for scrambler, differential encoder and FEC encoder will provide facility for selection of scrambler, differential encoder and FEC encoder respectively. BPSK/QPSK selection control will give the option for the selection of modulation type that we required. This data will be filtered by using RRC (root-raised-cosine filter) filter with roll off factor options of 20%, 25% or 40%. RRC filter outputs will be frequency translated by NCO, which will give 10 bit digital I and Q outputs [4].

5.1 Scrambler

A scrambler is a device that inverts the signals or encodes a message or data at the transmitter to make the message unintelligible at the receiver end. It manipulates a data stream before transmitting it through the channel. The manipulations or data are reversed or brought to the original form by a descrambler at the receiver side. Scrambling is widely used in satellite communications, radio relay communications and PSTN modems. The scrambler block can be placed just before a FEC coder, or it can be placed after the FEC, just before the modulation block.

5.2 Differential encoding

Differential data encoding modifies the raw digitized data by creating a secondary, encoded data stream that is defined by changes in the digital state, from 1 to 0 or from 0 to 1, of the raw data stream. This differentially encoded data stream is then modulated and transmitted. In differential data encoding, a change in a raw data bit's digital state, from 1 to 0 or from 0 to 1, produces a 1 in the encoded data stream. No change in digital state from one bit to the next, in other words a bit with a value of 1 followed by another bit with a value of 1 or a bit with a value of 0 followed by the same, produces a 0 in the encoded data. For instance, differentially encoding the data stream containing 01010011001010 renders 1111010101111.

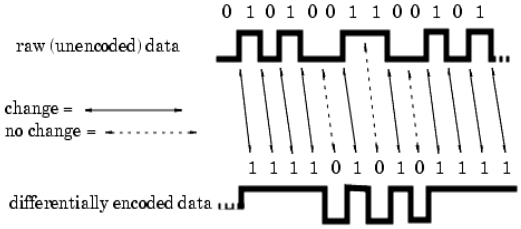

Figure-5 Differential encoding of data stream

5.3 Forward error correction

Forward error correction (FEC) is a technique used in data transmission for controlling errors over unreliable or noisy communication channels. The main purpose is the sender encodes their message or data in a redundant way by using an error correcting code (ECC). The redundancy allows the receiver to detect a limited number of errors that may occur anywhere in the message and often allows to correct these errors without retransmission. FEC filter gives the receiver the ability to correct or detect the errors without need of a reverse channel for the retransmission of data, but for this there must be a fixed, higher forward channel bandwidth. Therefore, FEC is applied in situations where retransmissions are more costly or impossible, like one-way communication links and when transmitting to multiple receivers in multicast systems. FEC information is generally added to mass storage devices for the recovery of corrupted data or message. FEC filters are widely used in modems.

5.4 Root-raised cosine filter

This filter is widely used to perform the matched filtering. It helps in minimizing the inter symbol interference. For the minimum ISI (Inter symbol interference), the overall response of transmitter filter, channel response and receiver filter must satisfy the Nyquist ISI criterion. This is the most popular filter response that satisfies this criterion. Half of this filtering is done on the transmitter side and the other half is done on the receiver side. On the receiver side, the channel response, if we can accurately estimate it, then it can also be taken into account so that the overall response is Raised-cosine filter.

6. SYNTHESIZED RESULT ON XILINX

Figure-4 BPSK/QPSK top level block

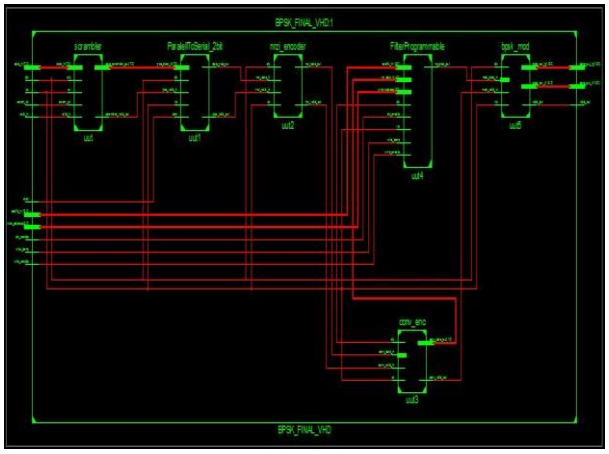

Figure-4 RTL Schematic of BPSK/QPSK Modulator

7. CONCLUSION

From this project, we can come to the conclusion that we can send the data stream or an analog signal from source to destination point using this modulator. This modulator includes two modulation techniques. Binary phase shift keying (BPSK), and Quadrature phase shift keying (QPSK). Modulation on the signal is applied within the modulator by adding the sine and cosine wave, which is being generated by DDS. The ideal speed of the transfer of the data stream is from 2.4 kbps – 2.048 Mbps.

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