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DFM Challenges and Solutions for 14nm FinFET

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ABSTRACT
In this Paper, advanced methods for DFM Verification and solutions are presented for lower nodes. It includes the need for Litho-Friendly Design, CMP aware Fill, Process Variation Issues and its impact on the design. Along with the DRC/LVS checks which deal with the physical verification processes, in lower technologies nodes, DFM should also be equally given importance as without it, it is impossible to achieve the silicon with maximum yield. Goal of DFM is to improve yield by minimizing defects like systematic, random and parametric defects through prevention, detection and fixing the hotspots.

Keywords
Design for Manufacturability (DFM), Litho Friendly Design, Critical Area Analysis, Via Optimization Solution & SmartFill.

1. INTRODUCTION
As we are moving towards advanced nodes, DFM hotspot checks is going to be key factor for yield improvement. At Lower nodes, our role is not only to make our design free from all DRC violations, but we have to make our design lithography friendly which can be printable on the real silicon by considering all possible variations in the fabrication process. DFM involves several steps for checking different kinds of hotspot or defects which can leads you towards lower yield and degraded performance. It is advisable to integrate DFM flow with placement and route flow, because certain patterns are no longer fixable post-tape out and it may lead you towards failure to meet market demand on time. In more when you are dealing with 3D FinFET structure, many parameters comes into picture which needs to be handled carefully, though 3D FinFET structure provides you good results in terms of power, area and performance. Due to compact poly silicon pitch, shrinking of channel length and innovative structure we have we have about 50% reduction in area. Performance gain is also nearer to 50%. If we use dual gate structure of FinFET, we will have less corner effect and we can reduce Ioff by 35%. Figure 1 shows the FinFET structure and also the comparisons of achievement over Power, Area and Performance [7].

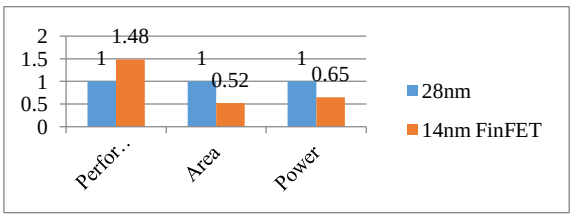

Fig. 1 14nm 3D FinFET Comparison with 28nm Traditional Planar

2. LOWER NODE CHALLENGES

2.1 Litho Friendly Design
At the time of sign-off if your design is DRC clean and on EDA tools it looks perfect having ideal rectilinear shapes with no opens or shorts. But it is not possible to fabricate exactly the same shapes as it looks like on your EDA tools. As we are transforming in advanced nodes, conventional light sources like KrF is no longer useful. ArF is useful only up to 16nm. For 10nm and beyond that we have to find some other light source having smaller wavelength like EUV technique. As of now we can use ArF as a light source for 16nm and 14nm with double patterning only due to the limitation of minimum distance which can be fabricated on the silicon. Lithography imperfections may results in the lower yield and reliability. Sometimes it may also affect to functional behavior of your circuit. Situation will be more hectic when you are not having clear open in your design and it passes through test and declared good. But when this passed chip goes into package and reaches to the end customer and you may have complained that your product is not working according to specified functionality. Double patterning technique also comes with some new challenges,

- Double patterning includes more numbers of DRC checks and complex design rules i.e. more than 2000 checks for 14nm. Figure 2 shows Same Mask spacing rule violation from Cadence Encounter tool.

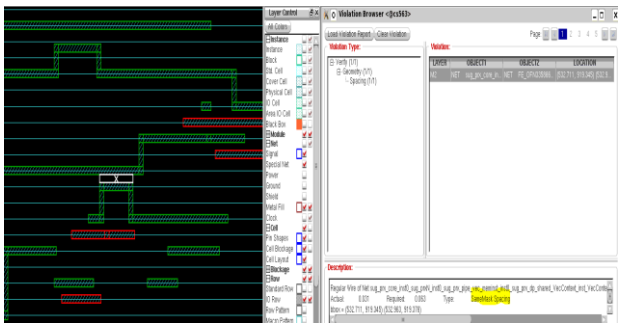

Fig. 2 Same Mask Spacing Rule Violation in Double Patterning

- Overlay error, increased numbers of lithography steps and increased cost are also headache in double patterning.
- Variation in parasitic due to different two masks creates major issue for analog and mix design engineers.
- We need to deal with color aware layout at each and every stage of physical design especially in placement as well as routing stage. For an example as show in Figure 2

during the placement of cell B, either we can put dummy space between both the cells or we can flip cell B. [10]

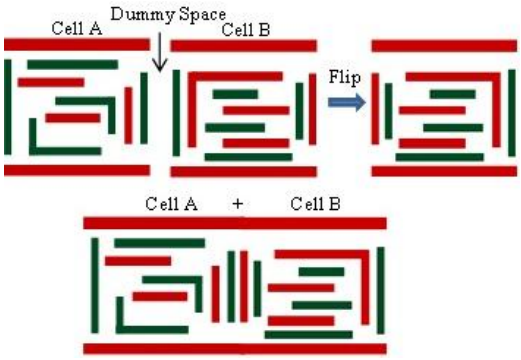

Fig. 3 Managing Double Patterning by Dummy Space or Flipping Cell

2.2 Silicon Manufacturing and Process Variation Issues

Defects like systematic, random and parametric occur during various manufacturing phases. Systematic defects are mainly related with layout design style, design rules and OPC techniques. Quality of Chemical Mechanical Polishing (CMP) process depends up on the planarity of the surface area. Sometimes due to various defects like oxide loss, dishing, erosion and total copper loss, we may not be able to maintain planarity, which results in manufacturing defects. Poly silicon is harder than metal, so in low metal density area, we will have dishing effects. Ideally we should avoid low density area for avoiding such kind of dishing effect.

Process Variations: Source and Impacts are shown below:

Table i. Various Process Variation Issues

Manufacturing Process	Circuit Parameters	Circuit Operations	CAD Analysis
Mask Imperfections	Channel Length	Temperature	Timing Analysis
Alignment, Tilting	Channel Width	Supply Voltage	RC Extraction
Focus, Dosage	Threshold Voltage	Aging PBTI/ NBTI	I-V Curves
Resist Thickness, Etch	Overlap Capacitance	Coupling Capacitance	Cell Modelling
Doping	Interconnects	Multiple Input Switching	Process Files
CMP			Circuit Simulations

2.3 Other Challenges

Reduced metal & poly silicon pitches creates some Layout Dependent Effects (LDE) like Well Proximity Effect (WPE), Shallow Trench Isolation (STI) effect, Poly Spacing Effect (PSE) and Oxide diffusion to Oxide diffusion Spacing Effect (OSE). Though local interconnects provides very high density contacts between lowest metal layer and base layer, it is also having very complex rules regarding dimensions and rectilinear shapes. In more there are some other challenges like open and shorts due to random particles at the time of fabrication process.

3. VERIFICATION

3.1 Lithography Variability Check

Once we have DRC clean layout GDS of our design we can perform lithography variability check. It will be performed on each & every metal layer, gate poly as well as dummy poly, oxide diffusion and via.

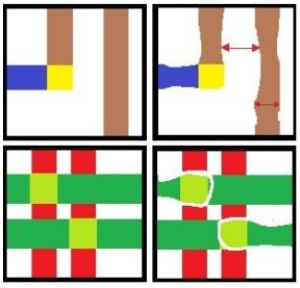

Fig 4. Lithography Process Checks

This process will be performed in three different steps.

As shown in Figure 4 there are different types of checks like minimum width check, minimum spacing check, minimum area check and minimum via enclosure check.

1. First define different process windows for printing of design with different parameter values like focus, dose, mask and bias.
2. Perform simulation for specified windows and detect potential hotspot which can create failures based on simulation results.
3. Calculations of manufacturing analysis score for each and every portion which shows how well your design can be fabricated on real silicon wafer. [6].

3.2 Critical Area Analysis (CAA)

CAA mainly deals with the defects which are supposed to be produced due to random particle at the time of fabrication in the foundry. CAA is going to be more complex and critical with new design rules for FinFET. There are two possible different scenarios. In one case, if two metal layers are close enough, there is possibility of short when a large size particle falls between two metal tracks as shown in Figure 3(a). In second case there is possibility that if random particle falls at the center axis of metal track, and size of the random particle is larger than metal width, it may create open, as shown in Figure 3(b). In both the case it creates failure, which gives you functional error which results in low yield [11]. With the use of EDA tool like Calibre Yield Analyzer we can detect the hotspot which can probably create open or shorts. CAA should be performed metal by metal. After having detecting this hotspot we can fix them by different techniques like metal bending, increasing space in critical area for avoiding shorts, which results in overall yield improvement. It is also advisable to perform re-run on the modified window to make

sure that we have not created any new potential hotspot by playing with physical dimensions of metal tracks [6].

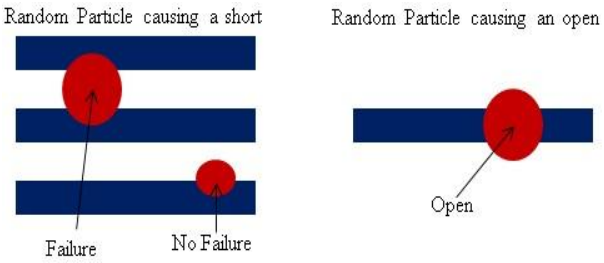

Fig 5 Critical Area Analysis (Bridging & Shorts creates failure)

3.3 CMP Hotspot Check

Planarity of your design directly affects your parametric as well as systematic yield. For achieving higher yield, model based planarity analysis plays very important role. By performing CMP model based simulation on your design you can detect potential planarity defects. By considering several factors rather than metal density, you can do metal filling in that area to for achieving higher level of planarity as well as yield, which will be discussed in the next section of this paper. Here we have suggested a flow for CMP hotspot detection. [6]

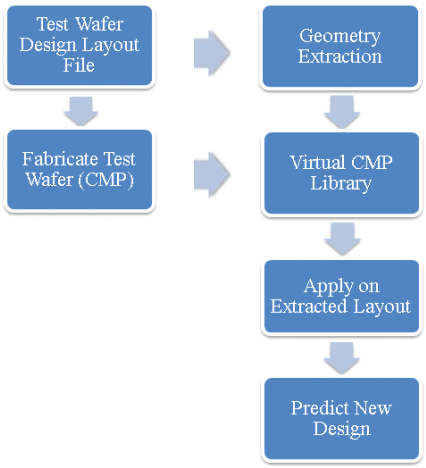

Fig 6.CMP Hotspot Check flow

First of all you have to prepare CMP process library for performing simulation process. For that you have to gather fabrication measurement data from a test wafer fabrication, which may be collected from your previous experience of fabrication. Once you have library for CMP simulation, you can apply it on your design for detecting CMP hotspot.

3.4 Manufacturing Analysis and Scoring

Manufacturing Analysis & Scoring is basically a grading system which replicates how good your design is in terms of DFM. Larger the MAS value, greater the yield. We have recommended rules which are technology specific and we call them design rule checks (DRC). But DRC is just a pass or fail type grading system. If we want analog scoring for our design, how exactly it can be fabricated on a real silicon wafer, MAS is the perfect grading system. It is based on recommended rules; priorities of recommended rules, standard deviation from their standard value; all such kind of things. Based on such type of analysis it will generate a MAS score for your layout which will help you to predict your yield and improving too. Figure 4 shows DRC v/s MAS grading system [7].

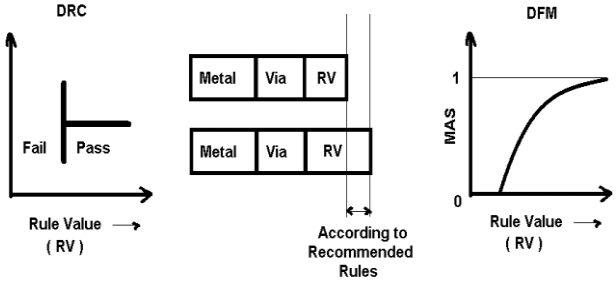

Fig 7 Manufacturing Analysis & Scoring

4. SOLUTIONS

4.1 Metal Filling with respect to RC analysis

In dummy metal filling, we only consider metal density variation throughout our design. But it is not sufficient especially when we are dealing with lower nodes due to innovative layout structure, 3D FinFET shapes and more numbers of metal layers. We have to develop some smart algorithms which perform RC extraction with the change in metal width or shapes; otherwise it will end up with timing failure of our design. In more there are some density constraints like minimum metal density, maximum metal density, density variation in nearby region as well as throughout your design. By considering all this you can perform more accurate metal filling which can give you higher level of planarity, results improved parametric yield of your design with no effect on your timing. [6].

4.2 Design Rule Check by Pattern Matching

Design rule check with the help of rule deck written in text file takes long run time. In more it is very time consuming and complex process to create that design rule deck, you have to specify each and every measurements very exactly. As shown in column chart for 14nm node you have more than 2000 design rule checks due to more complex 3D structure and low poly pitch. If we can identify all that patterns which always creates a problem you can create a library for pattern matching. It will directly compare your design with the patterns exist in the library and finds out all the patterns which can violate design rules. It will take very less time compared to rule deck based design rule check.

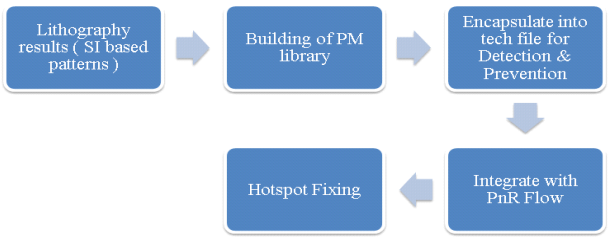

Fig 8 Pattern Matching Flow

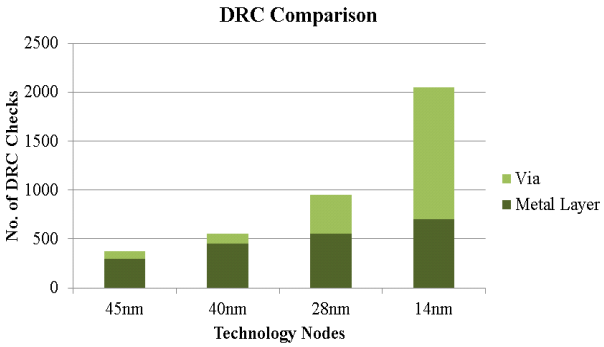

Fig 9 Numbers of DRC checks at different nodes

4.3 Via Optimization Solution

Via failure is one of the most dominating causes for lower reliability of your design. Due to the lithography variations there is possibility of power open or open if you have only single via structure. For better reliability of via we suggest doubling of via, insertion of via farm, sufficient sized via enclosure and via extension wherever it is possible in your design by considering congestion for particular metal layer. [7].

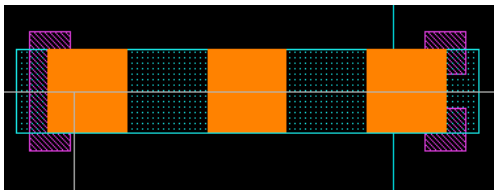

Fig 10 Via Optimization Techniques

5. FUTURE WORK

5.1 Extreme Ultraviolet (EUV lithography)

Imaging capability or minimum feature size of device is limited by the light source used in the lithography process. As of now we have been using Ultraviolet light source (ArF) of 193nm wavelength, we had started from 130nm and with the use of different smart fabrication techniques like double patterning, we have achieved feature size up to 16nm. But for advanced node like 10nm and beyond that UV light is no longer useful due fabrication process limitation. In more applied techniques like double patterning has been proven very costly due to more numbers of process steps as well as complexity for the same.

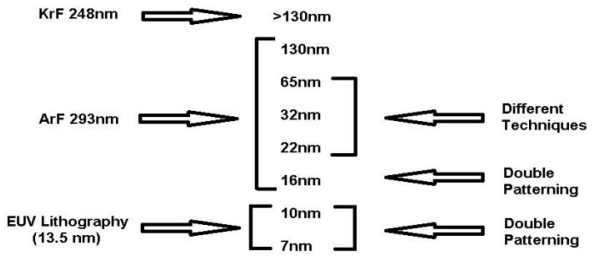

Fig 11 Lithography Roadmap

Extreme Ultraviolet light can be effective replacement of UV light source, which will reduce numbers of steps and complexity for the same. In Figure we have shown evolution of the light source and achieved feature size for the same.

5.2 Challenges with EUV

Major challenge for EUV based lithography is requirement of very high power source. For mass production on commercial bases it requires >1000W. But as of now it is limited up to only few hundreds, resulted in low throughput.

6. CONCLUSION

Advanced nodes provide you improved results in terms of power, area and performance at the cost of several challenges at DFM sides. Higher yield is the most important factor for any business unit and for that all this challenges needs to be taken care during the phase of designing as well as at the foundry. We should integrate DFM flow with our designing flow which will results in lower turnaround time and highly reliable products.

7. ACKNOWLEDGEMENT

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8. REFERENCES

[1] Debajit Bhattacharya and Niraj K. Jha, “FinFETs: from Devices to Architectures”, Vol 2014 , Article ID 365689, 21 pages, September 2014.

[2] Ruiqi Tian, Wong D.F, and Robert Boone, “Model based dummy placement for oxide chemical mechanical polishing manufacturability ”, Design Automation Conference, pp 667-670, 2000.

[3] Ritesh Turukhia, Mark Ward, S. K Goel, Brady Benware, “Bridging DFM Analysis and Volume Diagnostics for Yield Learning – A case Study ”, IEEE VLSI Test Symposium, pp 167-172, 2009.

[4] Ahmad Abdulghany, Rami Fathy, Luigi Capodieci, Piyush Pathak, Sriram Madhuvan, Shobhit Malik, “Smart Double-Cut Via Insertion Flow with Dynamic Design Rules Compliance for Fast New Technology Adoption”, unpublished.

[5] Robert Boone, Domenico Loparco, Fabio Melchiori, Matt Thompson, “Critical Feature and Improvability Analysis: An Effective Path to DFM Closure”, unpublished.

[6] Mentor Graphics Calire Design for Manufacturing related datasheets.

[7] KK Lin, Jeff Wilson, and Joe Kwan, “DFM Solutions for 14nm: Samsung and Mentor Graphics”, On Demand Webinar, Decemeber 2014.