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Comparative Analysis of Farrow Fractional Structure Rate Converter

Temidayo O. Otunniyi
Federal University of Technology, Akure
Computer Resource Center
Vice Chancellor's Office
Technology

Erastus O. Ogunti
Federal University of Technology, Akure
Dept of Elect/Elect
School of Eng & Eng Technology

Adedotun O. Owojori
Federal University of Technology, Akure
Dept of Elect/Elect
School of Eng & Eng Technology

ABSTRACT
Optimization of digital filter structure enhances its speed, reduces the filter length and filter coefficients which invariably lower the power consumption of the mobile devices. Reducing the filter operators as well as the coefficients reduces the filter redundancy. This improves the computational performance of the system in terms of memory utilization, bandwidth consumption and power usage. Farrow differential algorithm has improvement over the other existing algorithm such as farrow algorithm and differential algorithm. The algorithm was designed using Altera Digital Signal Processing tool box in MATLAB/ Simulink environment. When implemented it leads to reduction in the computational complexity, power consumption and silicon area. The decimation factor of 260 for a frequency range of 270.70 kHz was used. It also showed that a power gain of 83 dBm was observed as output for the poly-phase farrow differential algorithm compared to polyphase modified farrow with power level of 98dB and polyphase farrow algorithm with power rating of 140dB. Thus a remarkable lower power gain, lower complexity and lower power consumption in mobile system was obtained when compared to polyphase farrow polynomial algorithm and modified farrow algorithm.

Keywords
Farrow Differential algorithm, Modified Farrow, Farrow algorithm, Channelization, Multirate Digital Filter Bank, Software Defined Radio, Digital-Down Conversion

1. INTRODUCTION
The recent applications deployed on mobile devices have brought about wide usage of mobile phone or handset. These different applications such as Multimedia functionalities, Voice over internet and various data communication applications on different platform of the mobile devices have remarkable effects on their complexity and power consumption, therefore optimization of the filter structure realized is vital in the next generation mobile systems. Therefore it is pertinent to proffer solution to these major constraints limiting efficient/ optimized signal dissemination. Thus a good algorithm with low complexity and minimum power usage for efficient computation is required during extraction of channel of choice.

DSP computational systems involve multiplier-accumulator (MAC). It requires L multiplication and L-1 addition operations per sample to compute the sum of products (SOP) of the filter elements and forms N x N- bit multipliers which fuses with the accumulator. Full precision N X N bit product is 2N bits wide while the accumulator is designed to have extra K-bits in width. The arithmetic operation such as adders and multipliers consume much power which has significant effect on computational capability of digital filter. Conventional FIR filters with large filter taps operates with high sampling rate, which makes the filtering operation computationally expensive in terms of redundancy. Complexity reduction of FIR filter implementations has also been of particular interest since lower computational complexity leads to high performance.

Different algorithm has been proposed for reducing the hardware complexities. Most includes fractional sampling rate technique which are farrow interpolation filter, modified farrow filter, Taylor series approximation and the farrow differential interpolation filter methods as stated in [2, 8, 9, 10]. However, the Integer SRC with poly-phase decimator or poly-phase interpolator has proven efficient for lower complexity filter length and high interpolator rate.

The coefficients of Farrow Structure are fixed for a given order N and there is no need for updating the sub-filter co-efficient. The co-efficient of Farrow Structure determined the power consumption in dBm. Transposed Modified Farrow Structure (11, 12) with lower sample rate and low computational complexity. Modified Farrow structure (3) has been proven efficient for implementing rational sampling rate conversion (4), (3) by reducing the number of operator in Farrow structure. The complexity reduction can be achieved by changing range of delay parameter D so that the integer part of the coefficient is removed.

This paper focuses on farrow fractional channelization algorithm and farrow differential channelization algorithms and gives a model design of each and does a comparative analysis of both in terms of its computational complexity and power consumption.

2. RESEARCH METHOD
This technique uses super-heterodyne receiver architecture as a platform to demonstrate GSM signal processing, propagation, modulation and demodulation using different farrow algorithms as illustrated below and carry out proper estimation in terms of its complexity and power estimation.

The Global System for Mobile Communication (GSM) system uses the Frequency Division Multiplexing Access/ Time Division Multiplexing Access (FDMA/ TDMA) system; each physical channel is characterized by a carrier frequency

and a time slot number. GSM system frequencies include two bands at 900 MHz and 1800 MHz commonly referred to as GSM-900 and DCS-1800 (Eberspacher.*et al*., 2009). For the primary band in GSM-900 system, 124 radio carriers have been defined and assigned in two sub-bands of 25 MHz each in the 890-915 MHz and 935-960 MHz ranges, with channel width of 200 KHz.

In modelling the signal generation a stream of sampled speech data is fed into a source encoder in this case a Bernoulli random number is used which compresses the data by removing unnecessary redundancies.

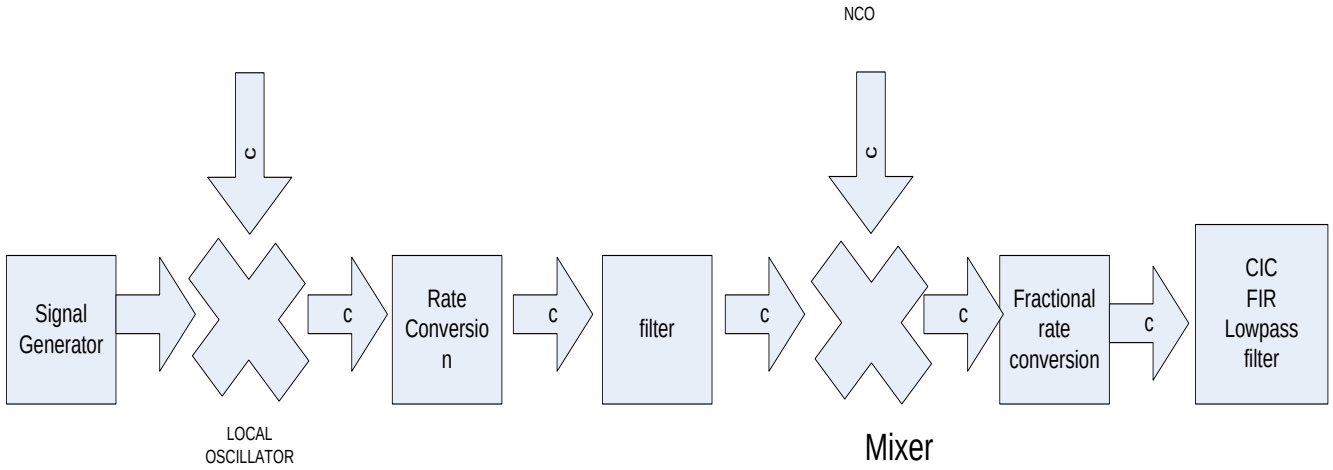

Fig 1: Block diagram of GSM digital receiver

The Bernoulli random number is probabilistic in nature with the probability equal to ½ and this gives an M-nary bit of 4. The sample frequency used is greater than twice the maximum signal frequency($f_m = 960$ MHz) according to Nyquist criterion. The resulting information bit sequence is passed to the channel encoder to add, in a controlled manner, some redundancy to the information sequence. This redundancy serves to protect the data against the negative effects of noise and interference encountered in the transmission through the radio channel.

GSM uses a combination of block and convolution coding with a convolutional rate of 1/2. Moreover, an interleaving scheme is used to deal with burst errors that occur over multipath and fading channels. This encoded and interleaved data are encrypted to guarantee secure and confident data transmission.

Finally the stream of bits is differentially coded and modulated using Gaussian Minimum Shift Keying (GMSK) due to its spectral characteristics and smoother phase shift. GSM uses Gaussian Minimum Shift Keying (GMSK) because of its smoother phase shift, and spectral efficiency. It is possible to estimate the number of bits in the transmission constellation that are been encoded, as well as the number of bits in each symbol and what the modems capacity will be at a given baud rate (baud/sec) or bd/sec using the following relation:

$b=\log_2(M)$

b = Rb/ B

for GMSK

(B*Tb) has values within 0.3 to 0.5

Rb = (bits/ symbol)*(symbol/ seconds)

Tb =1/ Rb

NB (1 symbol = a sec/ Hz)

using 0.3 value

B = 0.3/ Tb

$w_c = 2\pi f_c$

Where band efficiency b is the number of bits per symbol

M is the constellation or different symbol possible states

Rb is the bit rate or transmission rate in bit per second

B is the channel bandwidth

f_c Is the carrier frequency

The convolutional encoder converts the k- bit information message vector into N- bit channel input sequence dependent on the previous L-1 input into of the redundancy codes from the messages to form the code words.

Binary Convolutional Encoder with K (=2)-bits input and N (=3) - bits output and L -1 (=3) 2 bits registers having $2^{(L-1)K} = 2^{3.2}$=64 states.

Code rate = $\frac{K}{N}$

$$s_m(t) = A_{mc}S_{uc}(t) + A_{ms}S_{us}(t)$$

$$\mathrm{Re}\left\{(A_{mc} + jA_{ms})\sqrt{\frac{2}{T_s}}e^{j\omega_c t}\right\}$$

For m = 1, 2... M-1

$$A_{mc}\sqrt{\frac{2}{T_s}}\cos(\omega_c t) - A_{ms}\sqrt{\frac{2}{T_s}}\sin(\omega_c t)$$

For $0 \le t \le T_s$

$= A_m\sqrt{\frac{2}{T_s}}\cos(\omega_c t + \theta_m)$;

$= A_m = \sqrt{{A_{mc}}^2 + {A_{ms}}^2}$; $\theta_m = \tan^{-1}\frac{A_{ms}}{A_{mc}}$

$S_{uc}(t) = \sqrt{\frac{2}{T_s}}\cos(\omega_c t)$; $S_{us}(t) = \sqrt{\frac{2}{T_s}}\sin(\omega_c t)$

H=1/2 (modulating index)

T= bit duration

B = 3 dB bandwidth of shaping filter BT = 0.3 for GSM

Modulated Signal x(t) = $\cos(2\pi f_c t + \emptyset(t))$

$\emptyset(t) = 2\pi h\int_{-\infty}^{t}\sum_{-\infty}^{+\infty} a_k\left((s(\tau - KT)\delta(t)\text{---}\right.$

where a_k = binary data in bits (+/- 1)

Table 1: Sample values for Signal Generator during simulation

Input Seed	61
Sample Time	(1/1900e6 Hz)
Sample per frame	5
Output type	Double
Convolutional encoder	Polystrellis (7, 171,133)
BT Product	0.3
Pulse length	4
Symbol Prehistory	1
Phase Offset	0
Samples per Symbol	8

LNA is introduced so that the system can operate over possible or desired frequency range. It is used to adjust the gain and to scale down the power signal. The mixer is also introduced to translate the analog RF to Intermediate Frequency (IF) with the help of Local Oscillator by multiplying the incoming RF with LO. In this case the IF is set to 80 MHz at the same sampling rate of 2.5 GHz as the analog RF input. The use of a rate transition device helps to lower the sampling rate to 160 MHz This IF signal is further down converted to a second IF of 69.9 MHz corresponding to the IF of a commercial GSM but still at a sampling rate of 160 MHz which allows analog to digital conversion (ADC) and digital signal filtering to be employed to remove all the image and aliasing frequencies capable of distorting the signals and causing the IIP3 intermodulation [18] from the mixer.

The issues of ADC were problematic until the advent of recent semiconductor technology which brought hope into the future of sample digitization [1, 9, and 10]. The ADC for receiver requires 100 dB or more for the dynamic range characteristics. The higher the bit (B) of the ADC, the better the resolution of the signal been digitized.

The output of the ADC can be expressed below as a sum of weighted impulses.

$$x[n] = \sum_{k=-\infty}^{\infty} x(k)\,\delta(n-k)$$

The digital down converter (DDC) is an important component in any digital radio for performing frequency translation from 69.9 MHz to baseband. The convolved output of the input digital signal and the digital filter mixes with a numerical controlled oscillator (NCO) signal having a frequency f_{LO} of 69.9 MHz and sampling rate of 160 MHz to generate a sine, cosine or complex wave.

$$f_{NCO} = f_{BB} \pm f_{IF}$$

The NCO is capable of generating a multichannel real or complex sinusoidal signal depending on a real input IF signal. These NCO signals have independent frequency and phase in each output channel with amplitude of the created signal equal to 1 and the desired output frequency, F_0, generated as illustrated in [11, 12].

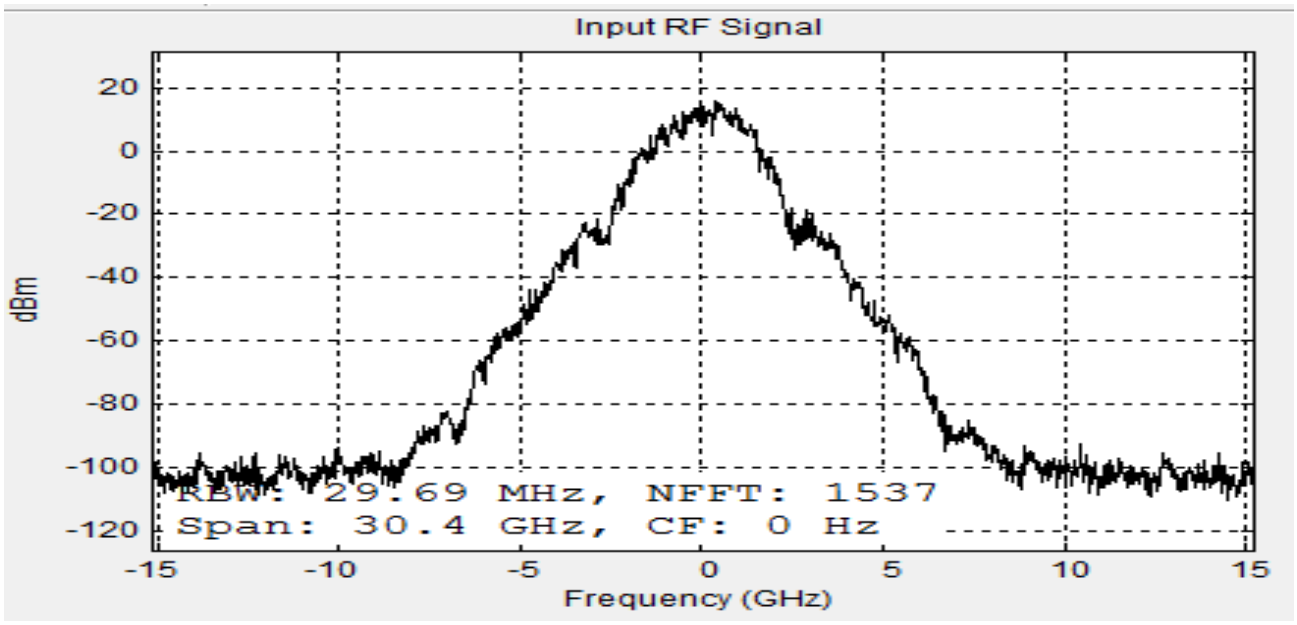

Fig 2: Input RF signal

Table 2: Sample Values of NCO

Phase Increment	5026454
No of dither bits	15
No of quantized accumulator bits	18
Output signal	Complex exponential
Sample time	1/80e6Hz

Table 3: Analog filter Sample values

Response Type	Low pass
Design Method	FIR Equirriple
Sampling Frequency	140MHz
Passband frequency	69MHz
Stop band Frequency	69.9MHz

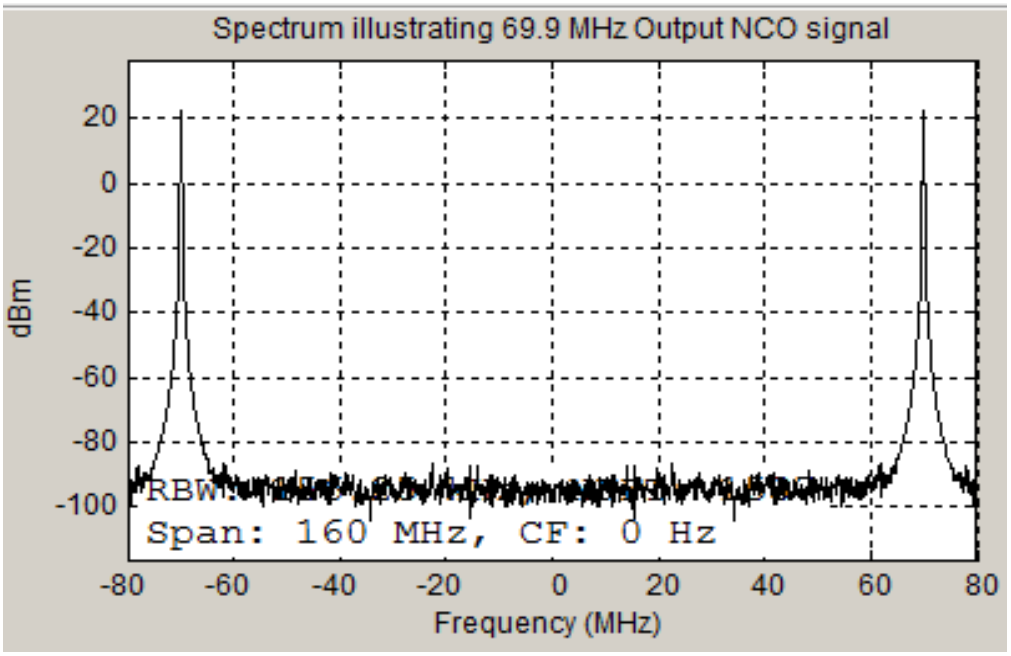

Fig 3: Spectrum illustrating the NCO output signal of 69.9 MHz

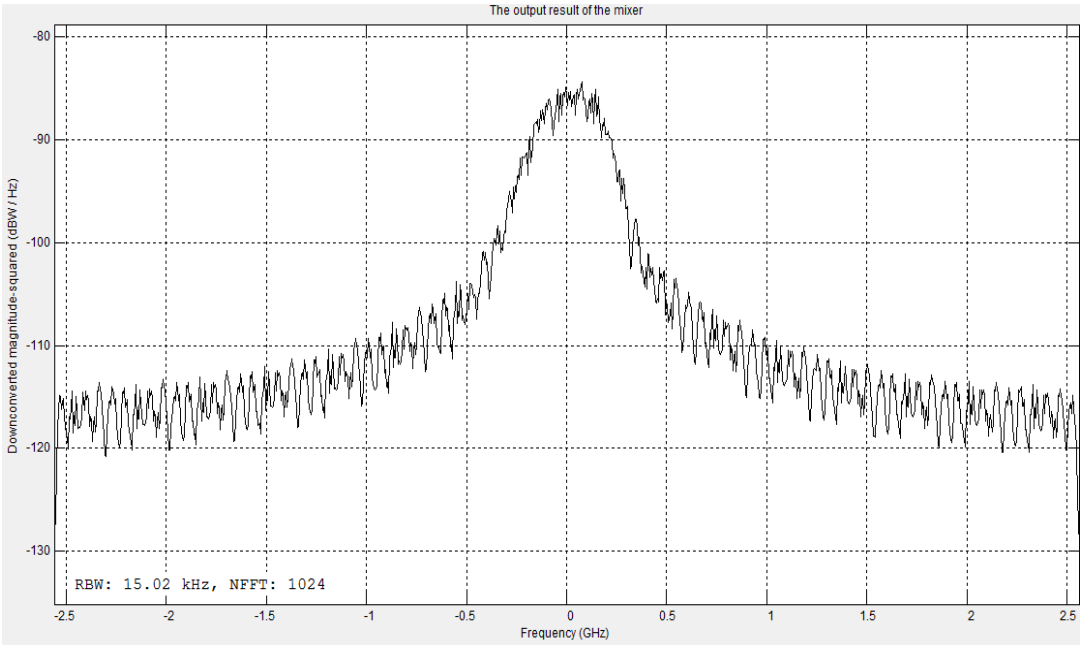

Fig 4: The output value of the mixer center around 0 M

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Polyphase Farrow Lagrange Interpolation Filter

At the digital front end, the sampling rate is at 160MHz. In other to reduce this rate to GSM commercial rate of 69.9 MHz, farrow fractional algorithms is required. The farrow filter relies on a filter bank structure whereby each filter coefficient is approximated as Nth order polynomial D [3, 4].

$$h(n,d) = \sum C_K\,(n)d^K, \text{ n=0, 1,----------, N.}$$

$$0 \le d \le 1.$$

The coefficients can be expressed in terms of the fractional delay d, that is $0 \le d \le 1$.

In Z- domain, the filter transfer function:

$$H_d\,(Z) = \sum_{n=0}^{N} h(n,d)\,Z^{-n}$$

$$=\sum_{n=0}^{N}\left|\sum_{k=0}^{p} C_k(n)z^{-n}\right| d^k \ldots\ldots\ldots\ldots\ldots(1)$$

$$=\left|\sum_{k=0}^{p} C_k(z)d^k\right|$$

Again the relation in (1) above suggests that the filter structure is made up of a bank of fixed weighted by the fractional delay d and summed at the output of every tap.

$$h(n,d) = \prod_{k=0,k\neq n}^{n} \frac{D-k}{n-k}$$

for n=0, 1 ,2, 3, ----------N

$$=(-1)^{N-n}\binom{D}{n}\binom{D-n-1}{N-n}$$

$$=\frac{D}{n}\times\frac{D-1}{n-1}\times\frac{D-n+1}{1}\times\frac{D-n-1}{-1}\times\frac{D-N}{n-N}$$

When N=1

$$h(n,d) = \prod_{k=0,k\neq n}^{1} \frac{D-k}{n-k}, \qquad for\ n = 0,1$$

$h(0,D) = 1 - D$

$h(1,D) = D$

When N=2 and a fractional delay d

$$(n,d) = \prod_{k=0,k\neq n}^{2} \frac{d-k}{n-k}, \qquad for\ n = 0,1,2$$

To calculate the coefficient

$h(0,d) = \prod_{k=0,k\neq 0}^{2} \frac{d-k}{0-k} = \left(\frac{d-1}{-1}\right)\left(\frac{d-2}{-2}\right)$

$=\frac{1}{2}(d^2 - 3d + 2)$

$h(1,d) = \prod_{k=0,k\neq 1}^{2} \frac{d-k}{0-k} = \left(\frac{d}{1}\right)\left(\frac{d-2}{1-2}\right)$

$=-d^2 + 2d$

$h(2,d) = \prod_{k=0,k\neq 2}^{2} \frac{d-k}{2-k} = \left(\frac{d}{2}\right)\left(\frac{d-1}{1}\right)$

$=\frac{1}{2}(d^2 - d)$

$H_d\,(Z) = \sum_{n=0}^{N} h(n,d)\,Z^{-n} = h(0,d) + h(1,d)Z^{-1} + h(2,d)Z^{-2}$

$=\frac{1}{2}(d^2 - 3d + 2) + (-d^2 + 2d)Z^{-1} + \frac{1}{2}(d^2 - d)Z^{-2}$

$C_0(z) = 1$

$C_1(z) = \frac{-3}{2} + 2Z^{-1} - \frac{1}{2}Z^{-2}$

$C_2(z) = \frac{1}{2} - Z^{-1} + \frac{1}{2}Z^{-2}$

$\overrightarrow{c(z)} = \varphi^T \vec{z}$

$$\overrightarrow{c(z)} = \begin{bmatrix} C_0(z) \\ C_1(z) \\ C_2(z) \end{bmatrix}$$

$$\varphi = \begin{bmatrix} 1 & 0 & 0 \\ -3/2 & 2 & -1/2 \\ 1/2 & -1 & 1/2 \end{bmatrix}$$

Following the fractional filter is the decimation by down sampling. Down-sampling the process that removes M-1 samples from the input-signal. If the input signal has frequency components outside the low-rate Nyquist frequency, aliasing will occur.

Hence, a low pass filtering as indicated in figure 5 below is used before the down sampling to avoid distortion of the signal $w(n)$ can be written as $w(n) = \sum_{k=-\infty}^{\infty} h(k)\,x(\text{n-k})$

$$\text{w}'(n)=\begin{cases} w(n) \\ 0 \end{cases}$$

$\text{w}'(n)= w(n)\left[\frac{1}{M}\sum_{K=-\infty}^{\infty} \text{e}^{j2\pi kn/M}\right],\ -\infty < n < \infty$

$\text{y(m)}= \text{w}'(Mm)= w(Mm)$

$\text{Y(Z)}= \sum \text{y(m)}\text{Z}^{-\text{m}} = \sum_{k=-\infty}^{\infty}(\text{w}'(Mm)\text{Z}^{-\text{m}})$

Where $\text{w}'(Mm)$ is zero except at instances of multiples of M

$\text{Y(Z)}=\sum_{k=-\infty}^{\infty}\left(\text{w}'(Mm)\text{Z}^{-\text{m}/\text{M}}\right)$

$=\sum_{k=-\infty}^{\infty} w(n)\left[\frac{1}{M}\sum_{K=0}^{M-1} \text{e}^{j2\pi kn/M}\,\text{Z}^{-\text{m}/\text{M}}\right]$

$\frac{1}{M}\sum_{K=0}^{M-1}\left[\sum_{k=-\infty}^{\infty} w(n)\left(\text{e}^{j2\pi kn/M}\text{Z}^{1/\text{M}}\right)\right]=$

$\frac{1}{M}\sum_{K=0}^{M-1}\left(w\left(\text{e}^{j2\pi kn/M}\text{Z}^{1/\text{M}}\right)\right)$

The transition bandwidth (ΔF) of the baseband signal is small compared to the sample rate fs (69.9 MHz), the order of the filter or number of coefficients is increased for accuracy and precision in word length effect and clock rate. In order to process this large number of coefficients with considerable word length processing and clock rate for a single channel filtering in a direct implementation by means of a conventional FIR filter, a lot of effort and high cost of multipliers would be required. To overcome this low-pass filter which does channel filtering on the baseband signal is combined with a down sampler (decimation) in a multi-stage pattern [13]

The multi stage decimation factor can be written as a product of individual decimation factor ($M = \Pi\, m_i = m_1 * m_2 * \ldots m_k$).

The total decimation factor can be calculated as:

$$\text{M}=\frac{fs_{\text{inp}}}{fs_{out}}$$

where fs_{inp} is the input sampling frequency from the ADC (69.9 MHz)

fs_{out} is the desired sampling frequency for the output signal (250 kHz).

The desired sampling frequency (250 kHz) is a function of the channel spacing of the GSM spectrum (0.1 MHz) in which according to Nyquist criterion should be twice the channel spacing. The total decimation factor equals 276.

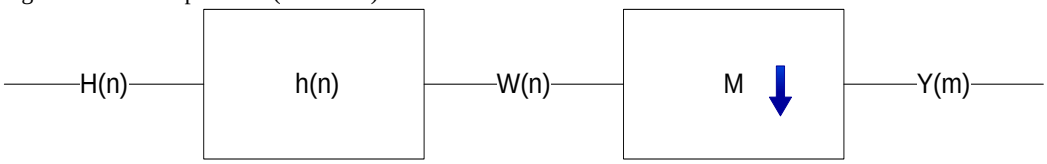

Fig 5: The decimator by factor M used in the design

The individual decimation factors for the multistage signal processing can be obtained using the equation below:

M1, optimum= $2M\frac{\left(1-\sqrt{\frac{M\Delta F}{2-\Delta F}}\right)}{2-\Delta F(M+1)}$

where ΔF = transition frequency and M is the overall decimation factor

For GSM, f_{sout} = 250 kHz;

$fsout\,/_2$= 125 kHz

$F_{pass=}$ 100 kHz

$F_{stop=}$ 108 kHz

Transition width $\Delta F = \frac{108-100}{108}$=0.074

M=$\frac{69.9e6}{250e3}$
=278

M1, optimum=$2M\frac{\left(1-\sqrt{\frac{M\Delta F}{2-\Delta F}}\right)}{2-\Delta F(M+1)}$=$2(278)\left[1-\sqrt{\frac{(278)(0.074)}{2-(0.074)}}\right]\approx$ 69

M=Π m_i =m_1 *m_2*….m_k). = 69,2,2 are the multistage decimator factors.

The common multistage low pass filter used is the cascaded integrator comb (CIC) and finite impulse response (FIR) filters which are used to filter as well down sample the baseband signal from 64 MHz to 250 kHz. The CIC filter is mostly used in the first stage of the sample rate conversion with the ability to carry out a high decimation rate change (Singh, 2009). A second low pass filter (inverse sinc) is included to compensate for the pass band droop caused by the sinc like response of the CIC.

The CIC- Filter (Cascaded Integrator Comb)

The CIC-filter is a multiplier free filter and use limited storage which is very good in an economical perspective. It was introduced by Eugene B.

$$\boldsymbol{y[n]} = \frac{\boldsymbol{1}}{\boldsymbol{M}}\sum_{\boldsymbol{k=0}}^{\boldsymbol{M-1}}[\boldsymbol{x(n-k)}]$$

If the average filter is removed, then the equation (1) will become

$$\boldsymbol{y[n]} = \sum_{\boldsymbol{k=0}}^{\boldsymbol{M-1}}[\boldsymbol{x(n-k)}]$$

This filter has unity coefficient and therefore requires little or no multipliers. This feature makes it very an efficient computational filter.

$$\boldsymbol{y[n]} = \frac{1}{N}\begin{cases}1, & for\ 0 < n < N-1\\ 0, & otherwise\end{cases}$$

Where N is the integer.

Y(Z)= $\frac{1}{N}\sum_{k=o}^{N-1} Z^{-k}$

Y(Z)= $\frac{1}{N}\frac{1-z^{-N}}{1-Z^{-1}}$

The frequency response of the CIC filter is shown below and is known as sinc function.

Y($e^{j\omega}$)= $\frac{1}{N}\frac{\sin\left(\frac{\omega N}{2}\right)}{\sin\frac{\omega}{2}}e^{jw[(N-1/2)]}$

Polyphase Modified Farrow Algorithm

It reduces the number of operator in Farrow Structure. The complexity reduction is achievable by changing the range of delay parameter D. This can be obtained by multiplying sub-filter coefficient matrix by transformation matrix T. It is a direct form of FIR filter structure

$$H_d\ (Z) = \left|\sum_{k=0}^{p} C_k(z)d^k\right|$$

Where d^k are the fractional delay coefficients and $C_k(z)$ are the Linear phase FIR.

$$\overrightarrow{c(z)} = \begin{bmatrix}C_0(z)\\ C_1(z)\\ C_2(z)\end{bmatrix}^T$$

$$\varphi^T = \begin{bmatrix}1 & 0 & 0\\ -3/2 & 2 & -1/2\\ 1/2 & -1 & 1/2\end{bmatrix}`$$

$$= \begin{bmatrix}1 & -3/2 & 1/2\\ 0 & 2 & -1\\ 0 & -1/2 & 1/2\end{bmatrix}$$

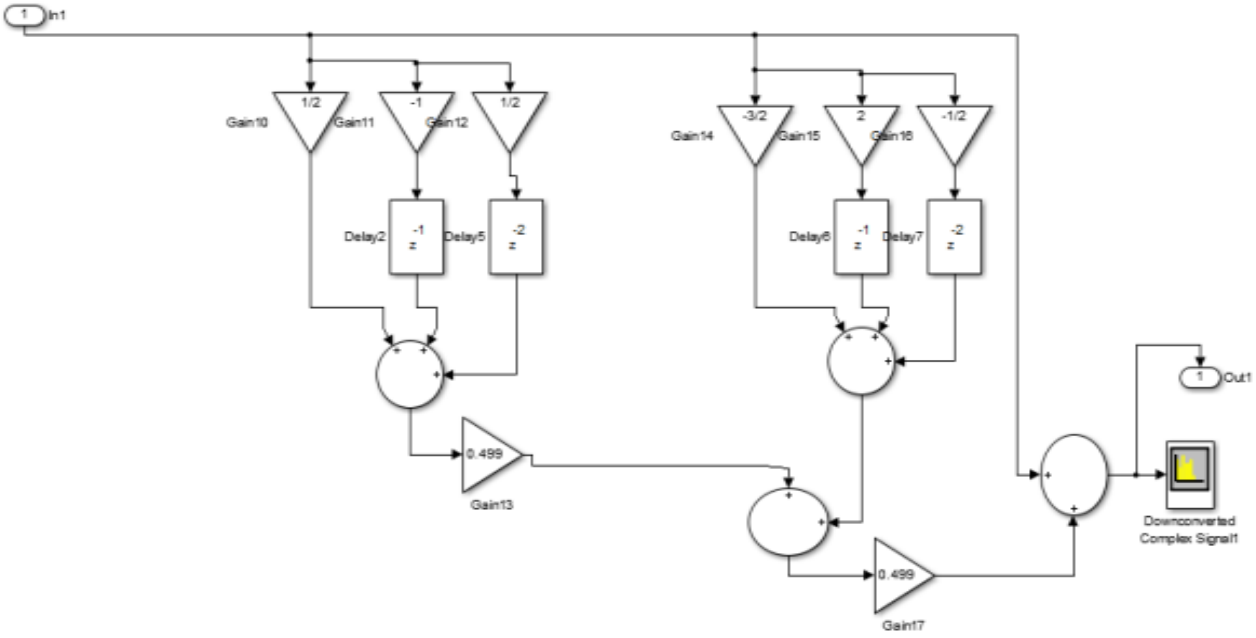

Fig 6: Polyphase Farrow structure

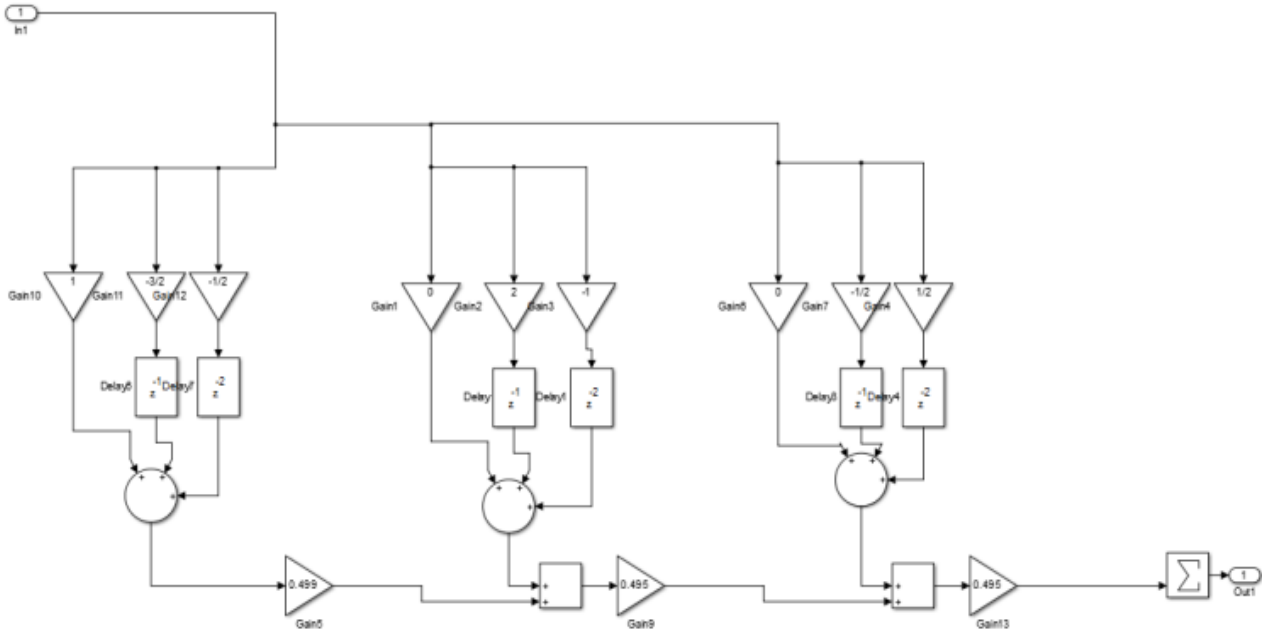

Fig 7: Polyphase Farrow Modified structure

Farrow Differentiating Interpolating Filter STRUCTURE

Farrow differentiating Interpolation filter provides another approach for implementing fractional delay filters using LaGrange polynomials. It uses piecewise approximation of the filter into a polynomial that shares a common set of coefficients. This result in interpolation of input signals. Two important design parameters are polynomial order (L) and Farrow sub-filter Length (N). Farrow differentiation filter is implemented as a direct form of FIR filter structure. It is obtained as approximation of continuous time function $X_c(t)$ by fractional delay D.

$$y(n) = h(d) * x(n)$$

$$y(n) = h(n,d) * x(n) = X(n-D) = \sum C_K D^K$$

The coefficients C_K are solved from the set of N + 1 Linear equation. This coefficients are expressed in terms of the fractional delays such that $0 \leq d \leq 1$.

$h(n)$ can be expressed as $C_0 + C_1 + C_2 + - - - + C_n$
Differentiating x(n)

$$D^V x(n) = \lim_{t \to 0} \sum_{k=0}^{\infty} C_K \; x(n-kt)$$

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Truncating $D^V y(n)$

$$D^V x(n) \approx \lim_{t\to 0} \sum_{k=0}^{\infty} C_K \;\; x(n-kt)$$

Removing the limit,

$$D^V x(n) \approx \sum_{k=0}^{\infty} C_K x(n)$$

Let $n = (n - D)$

$$D^V x(n-D) = \sum_{K=0}^{k} C_K \, x(n-D)$$

But $x(n-D)$ *are non integers delay sample of signal* $x(n)$

$$x(n-D) = \sum_{r=0}^{N-i} d^k \, x(n-D)$$

$$D^V x(n-D) = \sum_{K=0}^{P} C_K \sum_{r=0}^{N-i} d^k \, x(n-D)$$

$$= \sum_{r=0}^{N-i} \left[\sum_{K=0}^{P} C_K \;\; d^k \right] x(n-D)$$

Let

$$h(d)' = \sum_{K=0}^{P} C_K \;\; d^k$$

$$D^V x(n-D) = h'(d) * \mathrm{x}'(\mathrm{n})$$

The structure can be expressed in z domain as

$$H'_d \; (Z) = \sum_{n=0}^{N} h'^{(n,d)} \, Z^{=n}$$

$$= \sum_{n=0}^{N} \left| \sum_{k=0}^{p} C_k'(n) d^k \right| z^{-n}$$

Where $h'(n,d)$=
$C_0 \; + C_1 d^1 + \; C_2 d^2 + - - - + \quad C_n d^n = \left| \sum_{k=0}^{p} C_k'(n) d^k \right|$

The determinant of the equation above is called Vander mode determinant formed from $d_0 , - - d_n$

$$\mathrm{H}\,(d_0 , - - d_n) = \begin{vmatrix} 1 & d_0 & d_0^2 & d_0^n \\ 1 & d_1 & d_1^2 & d_0^n \\ 1 & d_n^1 & d_n^2 & d_n^n \end{vmatrix}$$

$\mathrm{h}'(d_0 , - - d_n) = C_k'(d - d_0)\,(d - d_1)\,(d - d_1)$-----
$(d - d_{n-1})$

$\mathrm{h}'(d_0 , - - d_n) = \prod_{i>i}^{n} \; (d_i - d_j)$
C_k' depends on the value of $d_0 , - - d_n$

Let

$$C_{k'}(n) = L_K(d)$$

This equation above can be rewritten as

$$\mathrm{h}(d_0 , - - d_n) = \; L_0(d)h(d_0) + L_1(d)h(d_1) +$$
$$\ldots\ldots\ldots\ldots\ldots + L_n(d)f(d_n) = \sum_{k=o}^{n} L_K(\mathrm{d})\mathrm{h}(d_k)$$

$$H_d \; '(Z) = \sum_{n=0}^{N} h'(n,d) \, Z^{=n}$$

The conceptual view of the farrow Differential algorithm is shown in Figure 8.

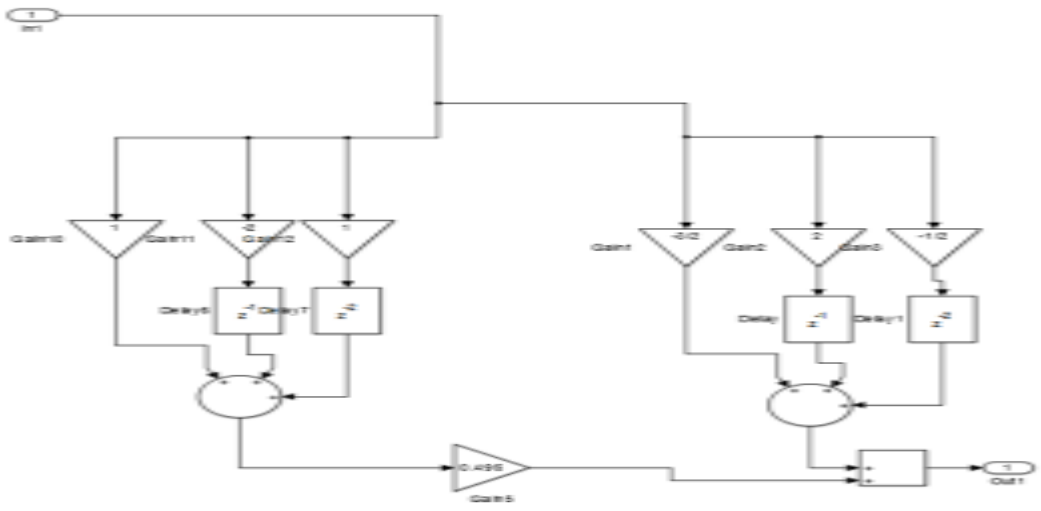

Fig 8: Conceptual view of farrow Differential algorithm

The digitized rate as shown in figure 4 above is set to 160 MHz, and the GSM sample rate is 69.93 MHz In order to convert the sample rate from 160 MHz to fractional sample rate of 69.93 MHz, the fractional rate conversion of 13/30 is required. Farrow differential algorithm is used to replace the normal conventional FIR filter. The digitized rare of 160 MHz is up-sampled by 13, followed by farrow differential interpolator filter and then decimated by down-sample of factor 30 with the fractional delay μ set to 13/30= 0.499. This set the new output sample rate at 69.93MHz. In order to take the signal to baseband, the new sample rate is decimated further by integer factor of 260 to get the output rate of 270 kHz.

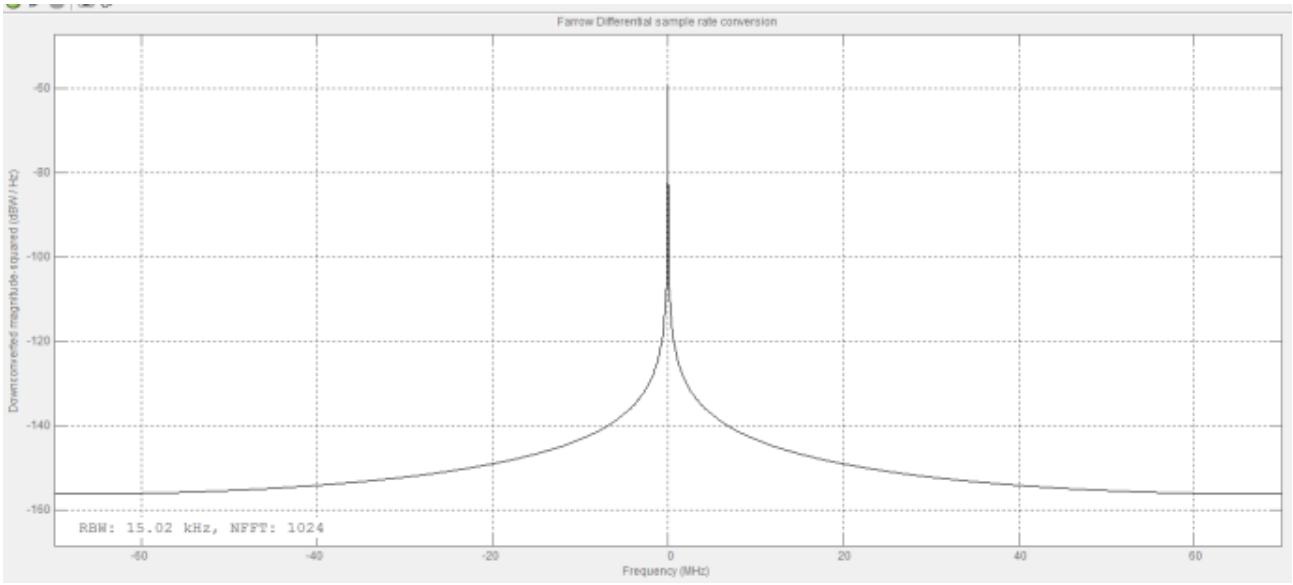

Fig 9: Polyphase Farrow structure

3. RESULTS AND ANALYSIS

In order to obtain all these results certain settings are observed on the MATLAB/ Simulink environment:

a. First, a DSP Builder 12.1 must be installed on MATLAB R2013a or better

b. In the Simulink environment, the data import/ export which will be saved on the workspace must have a structure with time format

The channel spacing of GSM is 0.2 MHz and to extract the desired channel from the wideband channel requires the passband and stopband to be set to 0.1 and 0.108 MHz to prevent aliasing**.**

CIC is designed to have a very large transition width $(w_s - w_p)$ because of its advantage of not having multipliers therefore, retaining most of the signals below its Nyquist frequency to be down sampled by m_1. The output of the CIC is further decimated with the transition width at the desired value i.e. between 0.1 MHz and 0.108 MHz

In the algorithms the computation complexity output is estimated in terms of the number of multipliers, adders, multiplication per input sample and addition per input sample of farrow filters used.

Polyphase farrow filter.

The complexity of polyphase farrow structure is given in terms of number of multiplier, number of adders, Multiplication per input sample and Addition per input sample

Number of Multiplier = 8

Number of Adders = 4

Multiplication per input sample = 6e8 multipliers per second

Power Consumption for farrow algorithm = 140 dB

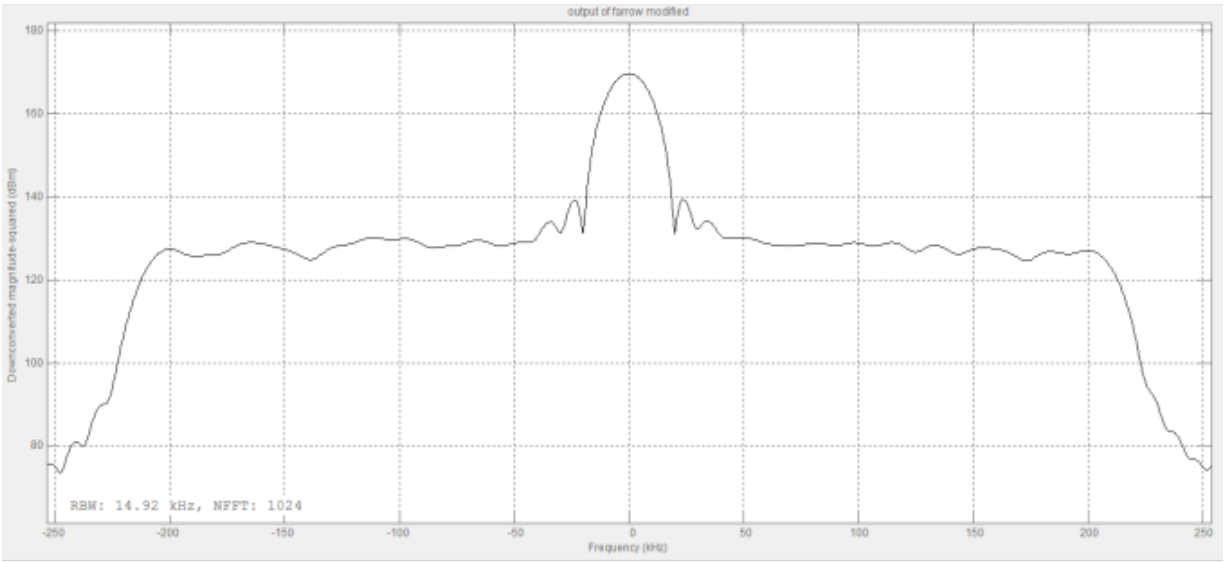

Figure 10: Polyphase Farrow structure decimation by 276

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Volume 2 – No.5, July 2015 – www.caeaccess.org

The output of the filter after decimated by a factor of 276 is shown below in figure 11.

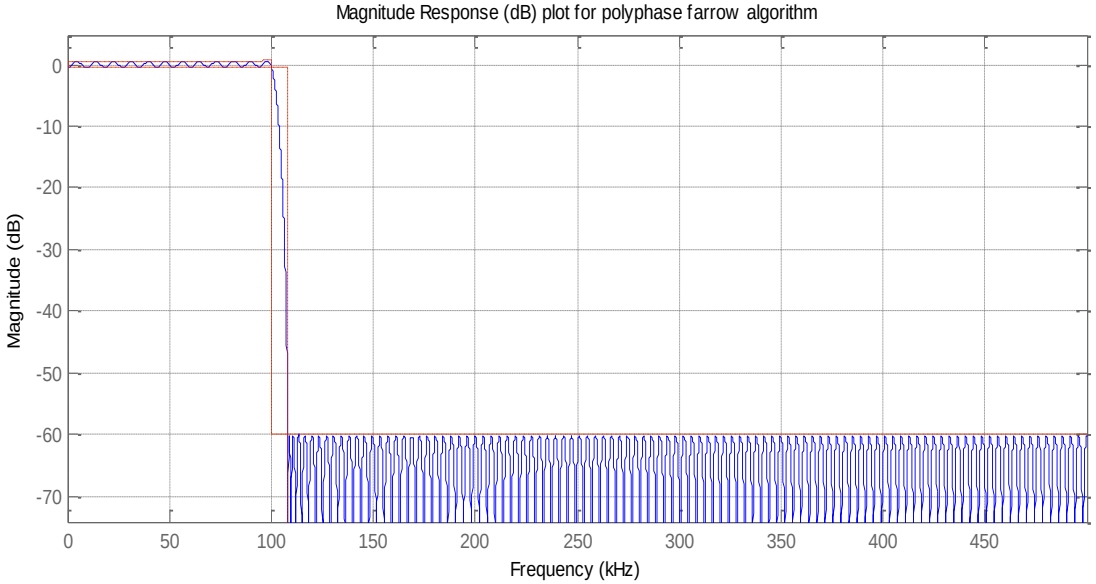

Fig 11: Farrow Structure Decimation by 276

Polyphase Farrow Modified filter

The complexity of polyphase Farrow Modified structure is given in terms of number of multiplier, number of adders, Multiplication per input sample and Addition per input sample

Number of Multiplier = 12

Number of Adders = 6

Multiplication per input sample= 8e8 multipliers per second

Power Consumption for farrow algorithm = 98 dB

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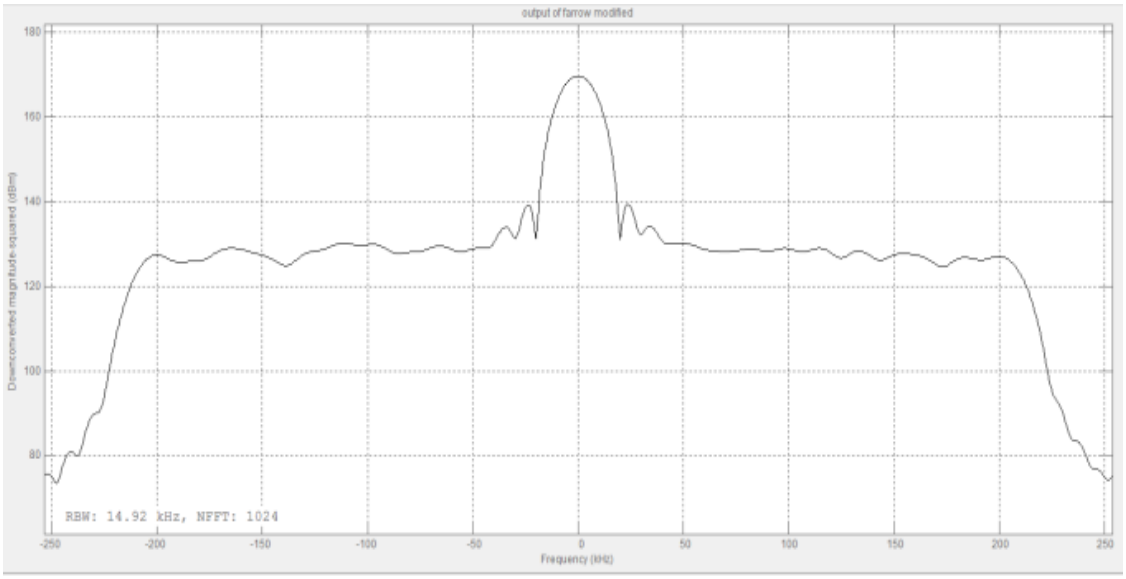

Figure 12: Farrow modified filter structure

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The output of the filter after decimated by a factor of 276 is shown below

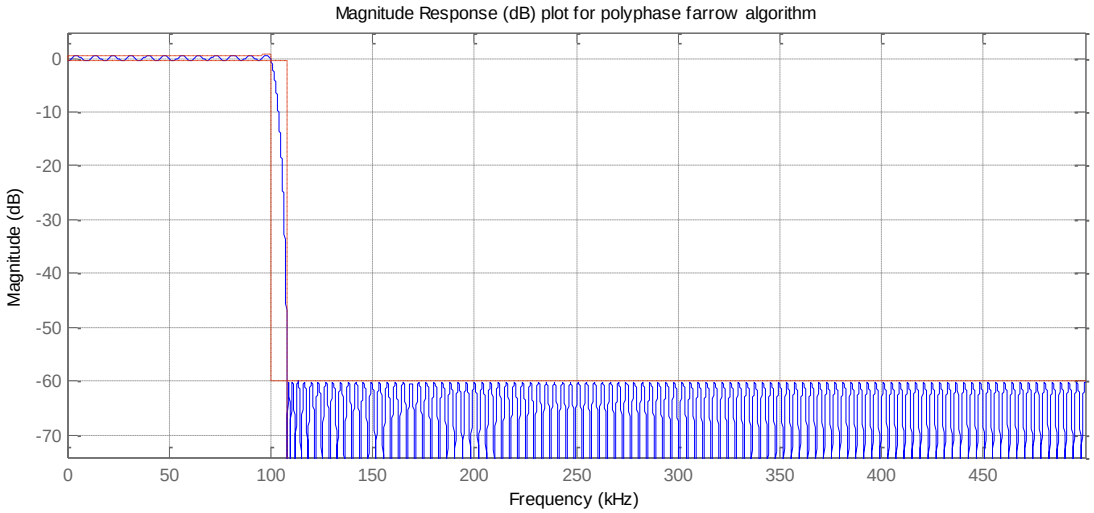

Fig 13: Farrow modified farrow structure decimation by 276

Polyphase Farrow Differential Filter

The complexity of polyphase Farrow Differential structure is given in terms of number of multiplier, number of adders, Multiplication per input sample and Addition per input sample

Number of Multiplier = 7

Number of Adders = 3

Multiplication per input sample = 8e8

Multipliers per second = 5e8 Multipliers per second

Power Consumption for farrow algorithm= 83dB

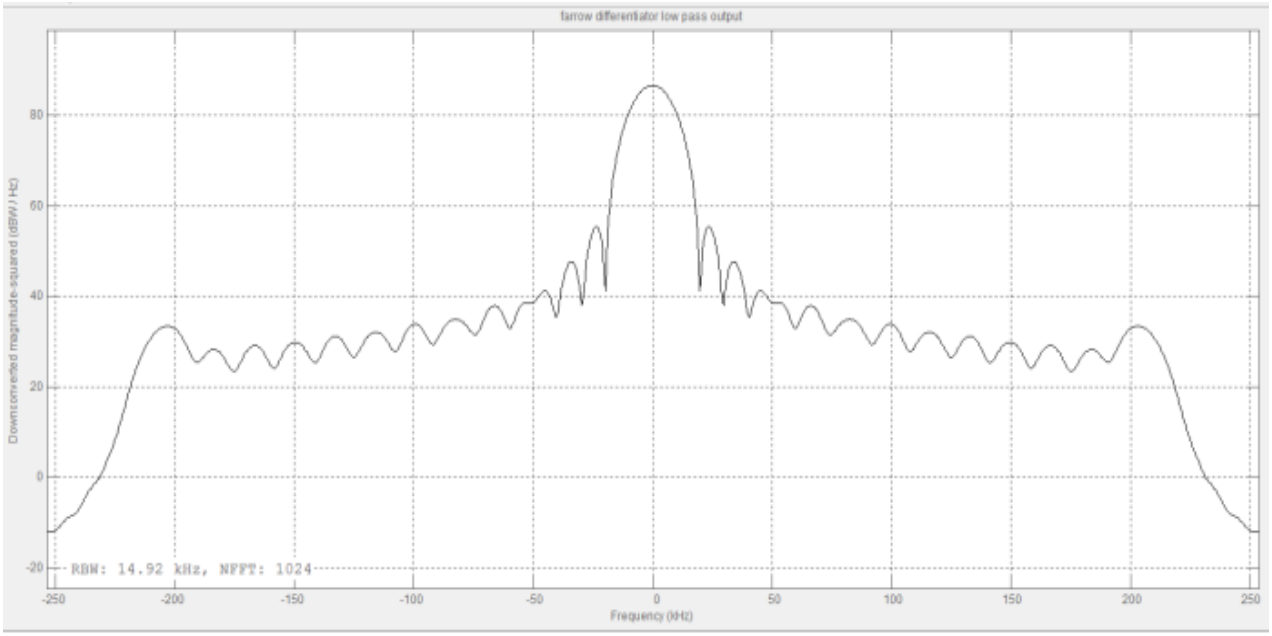

Fig 14: Polyphase Farrow Differentiator structure

The output of the filter after decimated by a factor of 276 is shown below

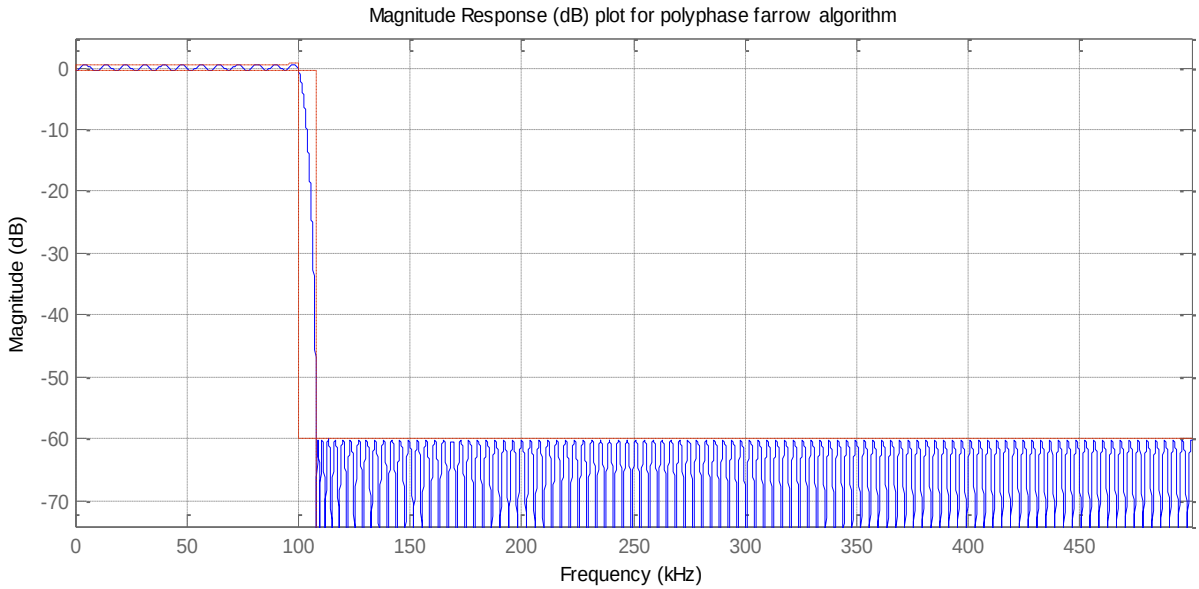

Fig 15: Farrow modified farrow structure decimation by 276

From this discussion so far, the farrow differential algorithm has the least computational task and the least power consumption rating as the number of required multipliers and adders are the least compared to the other two algorithms. The algorithm has reduced number of operators and thus it is computationally intensive and this has remarkable effect on its power consumption and the speed of its operation.

4. CONCLUSION

The computational implementation of farrow differential algorithms requires computational sharing of elements such as multipliers, adders and unit delays resulting in more efficient structure. The sharing of resources reduces the computational redundancy and reduces the cost of computational complexities, and hardware usage. These reduce the Central Processing Unit operation and memory usage and thus speed up the task.

Farrow differentiation interpolation polynomial is an approximation technique that yields exact values instead of round off values. The differentiation of the farrow filter leads to reduction in the coefficients generated and the number of multipliers and this leads to reduction in the complexity of hardware in digital systems in terms of silicon cost, area of hardware resources as in the case of FPGA, clock speed and power consumption

Farrow differentiation is suitable in areas where the fractional delay may change frequently from one SDR application to the next and this allows for great reuse of the hardware at minimum cost.

5. REFERENCES

[1] Rouphael, T.J. (2009). RF and Digital Signal Processing for software Defined Radio. Pp 371-375. Elsevier Inc.

[2] Farrow, C.W. (1988), A Continously Variable Digital Delay Element. 2641-2645. IEEE International Symposium.

[3] Laasko, T., Valimaki, V., Karjalainen, M. and Laine, U. (1996). Splitting the Unit Delay. IEEE Signal Processing Magazine. Vol. 13. Pp: 30-60.

[4] Valimaki,V, (2000) A new filter implementation strategy for Lagrange interpolation,"*Proc. IEEE Int. Symp. Circuits and Systems*, pp. 361–364,

[5] Hermanowicz, E. (2004), On designing a wideband fractional delay filter using the Farrow approach," in Proc. EUSIPCO'2004, Austria, Sep. 6–10, pp. 961–964.

[6] Farrow,C.W .(1988), A continuously variable digital delay element," in Proc. IEEE ISCAS'88, Espoo, Finland, 1988, pp. 2641–2645.

[7] Blok, M. (2005), Farrow structure implementation of fractional delay filter optimal in Chebyshev Sense, in Proc. SPIE, vol. 6159, Wilga, Poland, p. 61594.

[8] Harris, F. J. (1997), Performance and design of Farrow filter used for arbitrary resampling, in Proc. *DSP'97*, vol. 2, Santorini, Greece, 1997, pp. 595– 599.

[9] Hentschel, T., Henker M., and Fettweis G. (1999), The Digital Front- End of Software Radio Terminals, *IEEE Personal Communications*, pp 6-12.

[10] Ching-Hsiang, T. and Sun-Chung, C. (2006), Direct Down Conversion of Multiband RF Signals using Band Pass sampling, IEEE Transactions on Wireless Communicationsm Vol. 5, No 1, pp 72 - 76

[11] Johansson, .H and Lowenborg, P. (2003), On the design of adjustable fractional delay fir filters. Circuits and Systems II: Analog and Digital Signal Processing, *IEEE Transactions* on, 50(4):164– 169.

[12] Hakan Johansson. (2011), Farrow-structure-based reconfigurable bandpass linear-phase fir filters for integer sampling rate conversion. Circuits and Systems II: Express Briefs, IEEE Transactions on, 58 (1):46–50.

[13] Otunniyi T.O, Owojori A.O, Ogunti, E.O., Ponnle, A.A (2015): low complexity farrow differential channelizer algorithm. Communications on applied electronics 1(6): pp36-42, published by foundation of computer science, New York, USA

[14] Owojori A.O, Otunniyi T.O, Ogunti, E.O. (2015): Digital front-end for software wideband channelizer. Communications on applied electronics 1(6): pp36-42, published by foundation of computer science, New York, USA

[15] Mohammed, R. (2002), Multi- Rate Processing and Sample Rate Conversion. EE Times Home.