

Simulation of n-FinFET Performance Reliance on Varying Combinations of Gate Material and Oxide

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ABSTRACT

In this paper an n-type double gate FinFET at a gate length of 22nm is reported. Here the device performance of FinFET under different gate materials and also under different buried oxides is construed. Firstly, the drain current under different gate materials, with different work functions and SiO₂ being the buried oxide has been obtained. A transfer characteristic curve has then been obtained comparing the drain current for different gate materials at a given supply voltage of 0.5 V. Secondly, the transfer characteristic curve, comparing the drain currents obtained under different buried oxides at 0.5 V supply voltage with Aluminium being the gate has been obtained. And lastly obtained is the device performance for different combinations of gate materials and buried oxides and the results were compared. It can be inferred that, a metal gate and a high k dielectric is what gives a good performance at nanometre ranges. All the simulations have been done in Visual TCAD.

Keywords

Buried Oxide, Fin field effect transistors (FinFET), HfO₂ (Hafnium Oxide), Silicon on Insulator (SOI), TCAD.

1. INTRODUCTION

A MOSFET with more than one gate into a single device is referred to as a multi-gate device or transistor. FinFETs are one such multi gate device. The double gate FinFET has emerged as the promising technology for scaling the CMOSFETs to deca-nanometer range [1]. It also reduces the drain induced barrier lowering and improves threshold [2].

In FinFETs, the gate is wrapped around a thin, undoped Si, called as a 'fin'; this is from where it derives its name. The sides of the fin are wrapped around by an oxide (buried oxide), this breaks the active region into several fins and a gate overlaps the channel regions of the fins. This increases the electrostatic control of the gate over the channel and thus high switching ratios are achievable [3].

Figure 1 shows the schematic of a FinFET along with its important geometrical parameters, the gate length (L_G), fin width (W_{fin}) and fin height (H_{fin}).

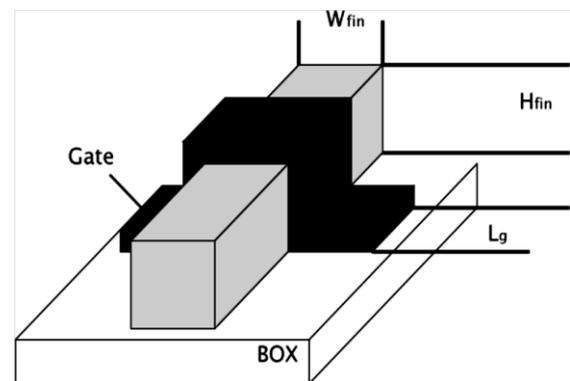


Fig 1 Schematic of a FinFET device, showing important dimensions: the fin width (W_{fin}), fin height (H_{fin}) and gate length (L_G) [3]

Traditionally, SiO₂ was settled upon as the buried oxide, and its thickness reduction enabled increase in number of transistors per chip, as proposed by Moore's Law [4] [5] [6]. But, however, to scale the FinFETs below sub-45nm range, metal gate electrodes and high k dielectric buried oxides are needed [7] [8]. As below this range the effective oxide thickness of SiO₂ is close to its physical limit and hence, results in high leakage current [9].

2. DEVICE FABRICATION

The circuit schematic of a 2D double gate n type FinFET in TCAD software is as shown in the figure 2. The modelling of double gate FinFET has been done in TCAD. TCAD is a software tool that models semiconductor fabrications and also semiconductor device operation.

FinFET has been fabricated on SOI (silicon on insulator) wafer with SiO₂ as the buried oxide of thickness 1nm. The gate length of the FinFET has been chosen to be 22nm. All the analyses have been done on this gate length only [10]. The substrate used is that of silicon. The gates as well as the source and the drain electrodes have been taken to be made of Al. The workfunction of both the front and back electrode is 4.17eV. Both the source and drain have ohmic contacts and the heat transfer coefficient is 1KW/K/cm².

Using nitride spacers leads to an increase in the on state current i.e. it improves the switching ratio [11]. Here four nitride spacers i.e. sp1, sp2, sp3 and sp4 have been utilised. A dual material spacer (the spacer with two different dielectrics e.g. silicon nitride and hafnium oxide) or triple material spacers (the spacer with three different dielectrics e.g. silicon dioxide, silicon nitride and hafnium oxide) can also be brought into use to further enhance the device performance [12].

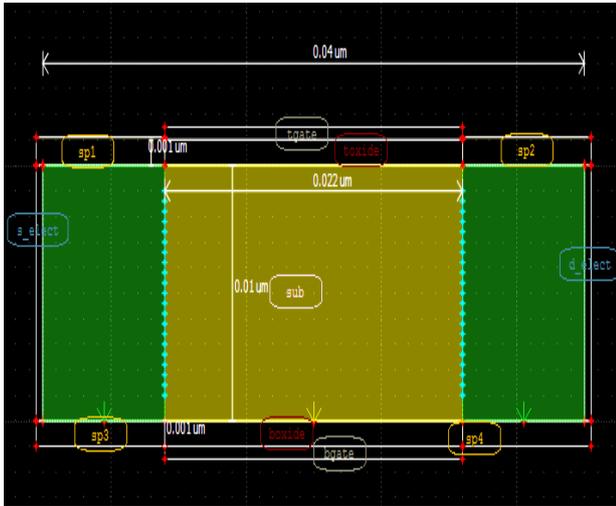


Fig 2 Circuit schematic of 2D FinFet in TCAD software

TABLE I Different Parameters at 22nm Technology

| Parameters | Dimensions |
|----------------------------------|----------------|
| Length of gate (L_G) | 22nm |
| Spacer Width | 1nm |
| Gate Oxide Thickness | 1nm |
| Thickness of Fin (W_{fin}) | Default (1 μm) |
| Doping Conc. Of Source and Drain | $1e+20$ |
| Doping Conc. Of Channel | $1e+18$ |

The height of the FinFET is 10nm. The substrate is doped with acceptor type impurity with the doping concentration of $1e+18/cm^3$, where as the source and drain are doped with donor type impurity with the doping concentration of $1e+20/cm^3$. The fin width has been varied from 1nm to 1000nm.

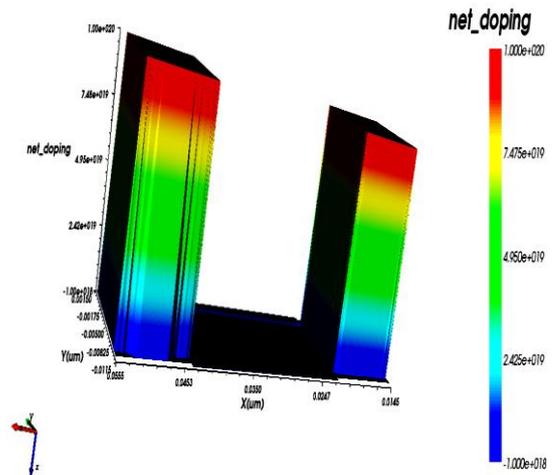


Fig 3 3D view of Net Doping in FinFET

3. SIMULATION AND RESULTS

Device simulations have been performed using the drift diffusion model at room temperature i.e. at 300K. Here different gate materials and buried oxides for an n-channel FinFET of gate length 22nm have been employed. For each combination of gate material and buried oxide, a set of results has been obtained and the transfer characteristics were then plotted and a comparison was made between them.

Firstly, only the gate material is varied, buried oxide remaining the same to be SiO_2 . Different materials such as Al, NPolySi, Cu, Au, Ag and Pt as the gate have been used, and the variation in the drain current as a function of firstly, the gate voltage keeping the drain voltage constant and secondly, the drain voltage keeping the gate voltage constant has been obtained. The supply voltage has been taken to be 0.5 V in both the cases. The obtained drain currents are then plotted against their respective gate and drain voltages and a comparison was made and studied (Figure 4 and 5). It has been observed, as shown in fig 4 and 5, that, the drain current was highest for NPolySi. Conventionally, polysilicon has been used in long channel MOSFETs as a gate material. But, Polysilicon is not favourable as gate material for smaller dimensional devices below 45nm because of its high thermal budget process; total amount of thermal energy transferred to the wafer during the given elevated temperature operation [13]. Because of its high thermal budget process, Polysilicon gate cannot be used when high k dielectrics are used as gate insulator.

Secondly, the impact of different buried oxide or (gate insulator) on 22nm gate length FinFET technology, has been obtained and studied. The model is that of drift diffusion and simulations have been performed at room temperature. We have obtained the transfer characteristics under three different insulators namely; SiO_2 , HfO_2 and Air. The gate is kept same to that of Aluminium and only the buried oxide is varied. The supplied voltage is taken to be 0.5 V. Here also the drain current as a function of gate and drain voltages respectively has been obtained. The drain and the gate voltages are varied from -0.5 V to 0.5 V one by one keeping the other one constant at 0.5 V. From the results obtained after simulations, transfer characteristics curve is plotted and a comparison is then made between the curves of that of different buried oxides (Figures 6 and 7).

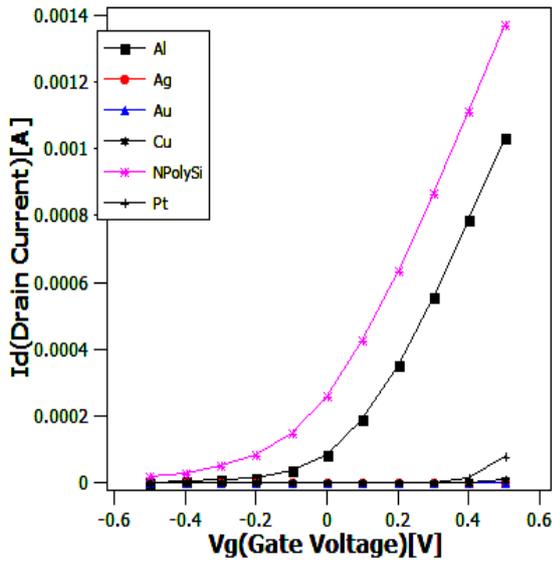


Fig 4 V_g versus I_d graph under various gate materials

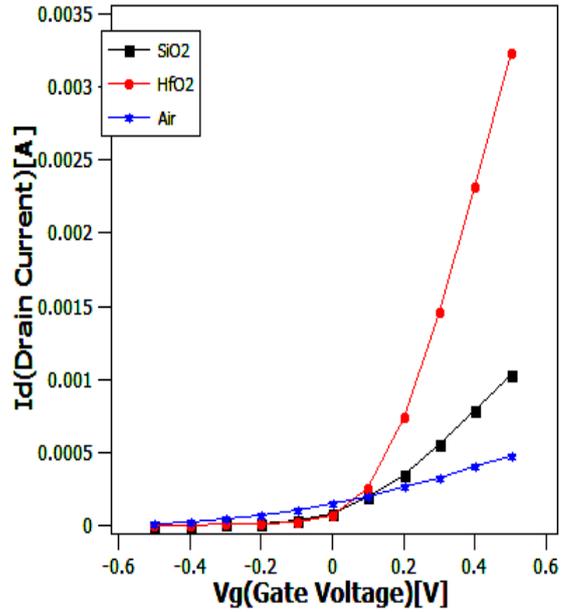


Fig 6 V_g versus I_d graph for different buried oxides at 22nm gate length

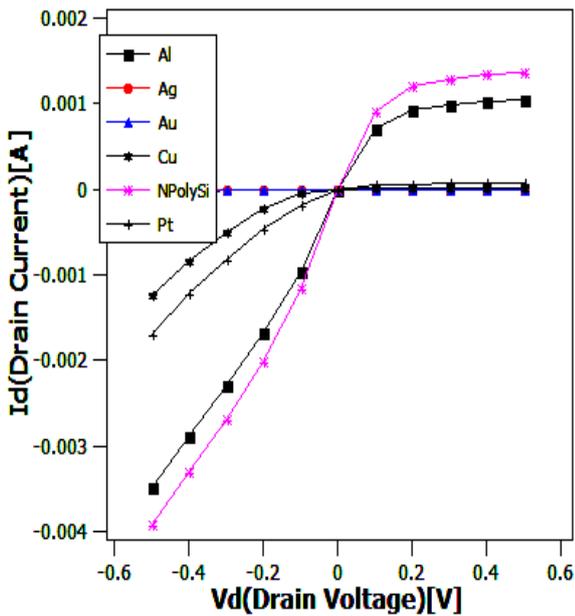


Fig 5 V_d versus I_d graph under different gate materials

It has been observed that for a given value of drain voltage or the gate voltage, the maximum drain current was obtained that for HfO_2 and then for SiO_2 and finally the minimum for Air. This is because the dielectric constant is highest for HfO_2 amongst the three and hence, it provides for better performance at high scaling with a low leakage current. Thus it can be said that HfO_2 is the preferred buried oxide.

Lastly, a combination of buried oxides and gate materials in an n channel FinFET at 22nm gate length has been used. The different combinations used are that of Al gate with SiO_2 as buried oxide, NPolySi gate with HfO_2 buried oxide, Al gate with HfO_2 buried oxide and NPolySi gate with SiO_2 as the buried oxide. The above materials have been utilized on the basis of the results obtained in the above two cases. After fabricating the FinFET with the above combination of gate material and buried oxide, simulation was done and the drain current was obtained as a function of gate voltage (varying from -0.5 V to 0.5 V) at a constant drain voltage of 0.5 V (Figure 8).

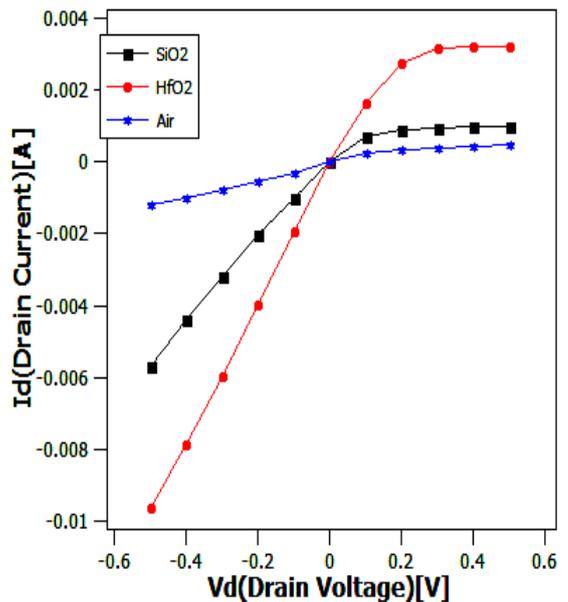


Fig 7 V_d versus I_d graph for different buried oxides at 22nm gate length

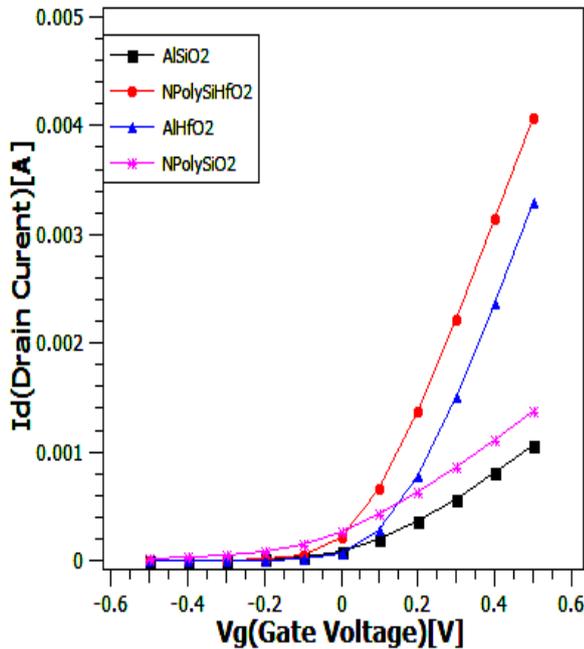


Fig 8 V_g versus I_d plot for different combinations of gate material and buried oxide

It has also been observed that the best transfer characteristics were obtained for that of NPolySi gate and HfO_2 buried oxide followed by Al gate and HfO_2 buried oxide. This owes to HfO_2 's high k which restrains the leakage current.

4. CONCLUSION

A 22nm gate length FinFET has been fabricated and analyzed in 2D using the Visual TCAD software at a supply voltage of 0.5 V. The transfer characteristics of the FinFET under different combinations of gate material and buried oxide have been obtained and a comparison between the obtained transfer characteristics has then been drawn. For nanoscale FinFETs, the gate is preferred to be a metal gate while a high k dielectric buried oxide is needed to combat the short channel effects. Accordingly, it can be observed that high device performance is achieved using aluminium as the gate and HfO_2 as the buried oxide. HfO_2 gives a good device performance owing to its high k value which can be as high as 30. It has also been observed that though, NPolySi as a gate gives a good device performance, but at nanoscale range Al is preferred because the former requires high temperature processing when used with high k dielectrics.

5. FUTURE SCOPE

As silicon devices scale down to atomic-scale limits, they are running out of ways to increase performance and lower power consumption and therefore new ways need to be devised. One such example is discussed in this paper. Integrating higher performance materials with silicon, such as III-V transistor channels that provide higher carrier velocity and higher drive current, helps enable continued scaling beyond the capabilities of silicon alone [14]. Also introducing Ge into the Si substrate helps improve the speed of transistor operation [15].

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