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Optimizing Current Characteristics of 32 nm FinFET by Controlling Fin Width

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ABSTRACT
The FinFET transistor structure assures to rejuvenate the chip industry by rescuing it from the short-channel effects that limits the device scalability endured by current planar transistor structures. In this thesis, we report the design, fabrication and physical characteristics of n-channel FinFET with physical gate length of 32nm using visual TCAD (steady state analysis). All the measurements were performed at a supply voltage of 1.5V and 5 nm oxide thickness. We report the drain saturation current is 0.0343453mA at Vg=1V and 0.0410523mA at Vg=1.5V which indicates approximately 20 percent hike in Id with increase in 0.5V gate voltage. We simulate the device for distinct fin thickness from 5 nm to 50 nm. In this thesis we report, for 32 nm gate length FinFET having above 21.33 nm fin width would consequence in short channel effects in spite of having high drain current.

Keywords
CMOS; silicon-on-Insulator (SOI); double-gate; Fin field-effect transistor (FinFET); tues gate; Drain Induced Barrier Lowering (DIBL).

1. INTRODUCTION
SOI (silicon on Insulator) basis multi-gate transistor structure is advisable for miniaturization of transistors and adequate for conquering short channel effects [1]. Fragile structured SOI devices are encouraging for escalating CMOS devices into nano-scale regime. One of them is dual-gate FinFET, includes a steep Si fin restrained by self-aligned double gate [2]. The FinFET technology is enticing because the procedure is accessible to implement with existing processing approaches [3]. The technology consists of developing a slender silicon island (fin) by engraving the silicon film [3].

Some of the essential aspects of FinFET are ultra thin Si fin for elimination of short channel effects, lifted source/drain to cut down parasitic resistance and revamp drive current [2]. FinFETs exploit symmetric gates to achieve tremendous performance, but can be fabricated with asymmetric gates so as to target threshold voltage [4]. FinFETs are drafted to benefit numerous fins to attain larger channel widths [4, 5]. Source/Drain pads bridge the fins in parallel. Increment in number of fins leads to boost the current through the device [4, 5]. For example, a device having five fins has five times higher current than single fin device [4]. The leading asset of the FinFET is the ability to exceptionally lower the short channel effects [2, 3, and 4]. In spite of double gate structure, the FinFET is related to its essence, the conventional MOSFET in layout and fabrication [2]. Three dimensional FINFET design is shown in Fig. 1. FINFET comprises a narrow perpendicular fin placed on the exterior of the wafer. Source and drain are crosswise on both sides of fin. This structure is positioned on SOI substrate.

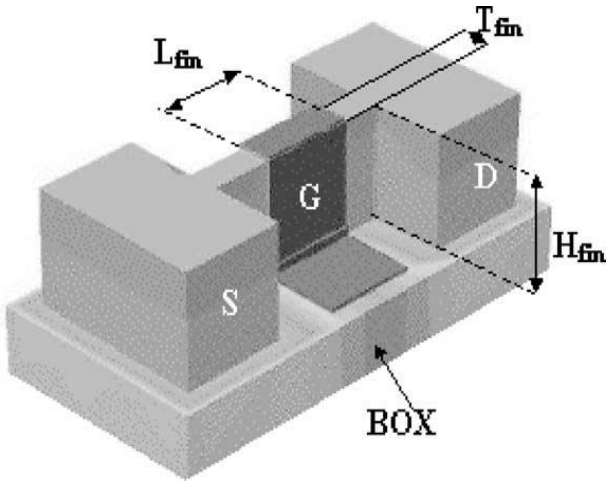

Fig. 1 FinFET structure [3]

2. DEVICE FABRICATION
The FinFETs are manufactured on bonded SOI wafers with a modified planar CMOS mechanism. A considerable discrepancy between a FinFET and a traditional planar FET is a slim active region (fin) [6]. Contraction of the fin width (i.e. body thickness), T_{fin} is essential for scaling of double-gate FinFET [6]. And the super-imposition of the gate to the active region should be productively restrained to curtail the transistor performance variation [6].

In two-gate FinFET, effective gate length equals to $2H_{fin}$ and in Tues gate FinFET equals to $2H_{fin} + T_{fin}$. Tues gate FINFET has two gates positioned on both faces of the fin resolved by H_{fin} and a gate raised above which is as much as T_{fin} [1, 7]. Accordingly, the gate length of 32 nm and H_{fin}=5 nm the calculated width of gate i.e. T_{fin}= 22nm. The top view drawing of FinFET is shown in Fig. 2.

Fig. 3 shows the material used for the contrasting regions. Nitride spacers (sp1, sp2, sp3 and sp4) are used as gate insulator and the gate oxide (toxide/Boxide) is SiO_2 type [1, 3, and 8]. The front and back gate electrodes are of aluminium metal with gate contact having work function of 4.17eV. The source and drain are homogenous having ohmic contact with

aluminium electrode. This region of the device is massively doped to 7e20 cm^{-3} of n-type ions and acceptor region is doped with 1e16 cm^{-3} p-type ions. The doping profile of the device is shown in Fig. 4. For simulation purpose, we build a mesh for the device to be fabricated according to the mesh size as given in table1; the meshed device is shown in Fig. 5. The steady state analysis of FinFET is realized by basic drift diffusion equation method [1]. The IV characteristic curves are simulated at room temperature (300K) for heat transfer coefficient of 1KW/K/cm^2. Fig. 5 shows the hole current in FinFET at Vg=V_d=1.5V and Drain current of 0.0410523mA.

Table 1 Regions of FinFET with mesh size

Region	Material	Mesh size(µm)
Substrate	Silicon	0.005
Source/Drain	Al	0.001
Tgate/Bgate	Al	0.001
Toxide/Boxide	SiO_2	0.0005
Spacers(sp1,sp2,sp3,sp4)	Nitride	0.1

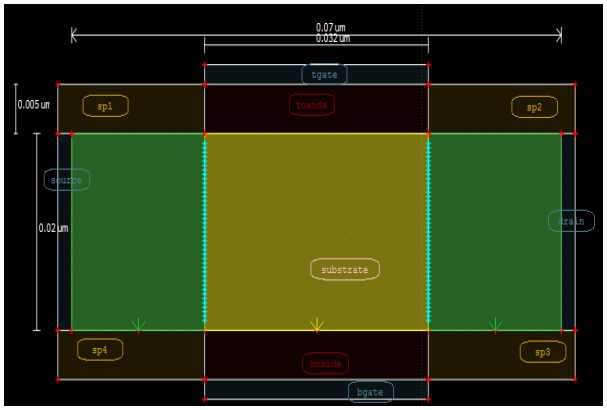

Fig. 2 Drawing of FinFET in TCAD

3. DEVICE CHARACTERISTICS

The emblematic trait of the FinFET is that the conducting channel is encased by a slender silicon "fin", which forms the body of the device. The thickness of the fin deduces the effective channel length of the device. The Wrap-around gate structure yields a superior electrical regulation over the channel and thus aids in reducing the leakage current and conquering other short-channel effects. Fig. 7 and Fig. 8 shows the I_d-V_d characteristics at 32nm gate length device with a 22nm-thick Si fin body on linear and logarithmic scale respectively. At 1.5V gate voltage, Drain voltage is varied from 0 – 1.5V with step of 0.05V. Following I_d-V_d characteristics are determined for different gate voltages (1.5V, 1.25V, 1V, 0.5V). The slope of I_d-V_d curve is higher for the high applied gate voltage. Fig. 9 shows the sub threshold I_d – V_g characteristics curves where V_g = -0.5 to 1.5V provided drain voltage of 1V and 0.05V.

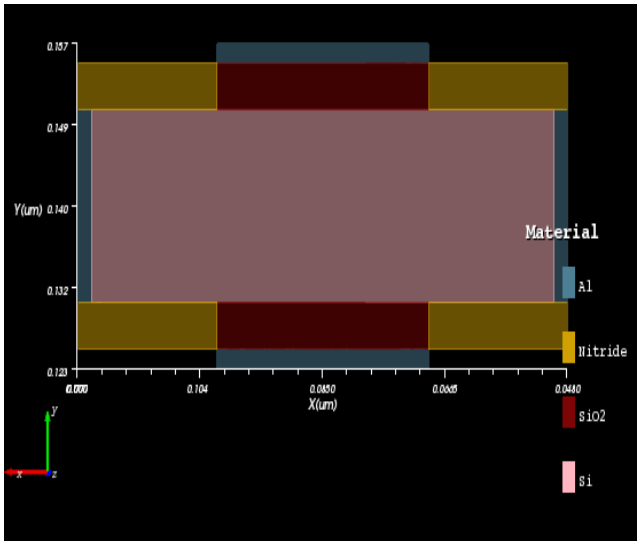

Fig. 3 Material used for fabrication

The effective width of the device is summation of top wall and two sidewalls of the Fin [1, 7] and in this simulation we are varying the top wall width while the sidewall width is fixed as its height of fin. As IC technology is shrinking according to Moore's law, here scaling of fin width is shown. Slender fin structures have detrimental impact on channel mobility due to supplementary scattering mechanism anticipating from side wall roughness [9]. Fig. 10 shows the fin width scaling from 50nm to 5nm, slope of I_d – V_d curve is reduced as a greater percentage of carriers are prone to scattering from sidewall. Thus the deterioration is worsened with contraction of fin width.

From Fig. 11 we can elucidate that FinFETs with wider fin thickness show improved performance regarding drain current, as FinFET thermal complications are further exacerbated with smaller fin [10]. In addition to excellent electrostatic characteristics are equipped by FinFETs, they undergo significant self-heating. The meager and confined dimensions of the fin lowers the thermal conductivity (which increases the thermal resistance) of the device due to diminished mean free path [10]. As heat convey out of the device is blocked, and there is hike in device's temperature. For the FinFETs, it is the temperature of the source that encounters the propagation of current [10, 4]. Hence wider fin has valuable impact on drain current but has constraint too. DIBL (drain induced barrier lowering) rises with increase in fin width. In case of wide silicon film devices, source/fin and drain/fin junction capacitance curtails. Hence drain electric field reduces the barrier of channel. When the drain and source proximity is consistent, then control of gate over channel region deteriorates with increased in channel volume which aftereffects in high sub-threshold swing with fin thickness [11].

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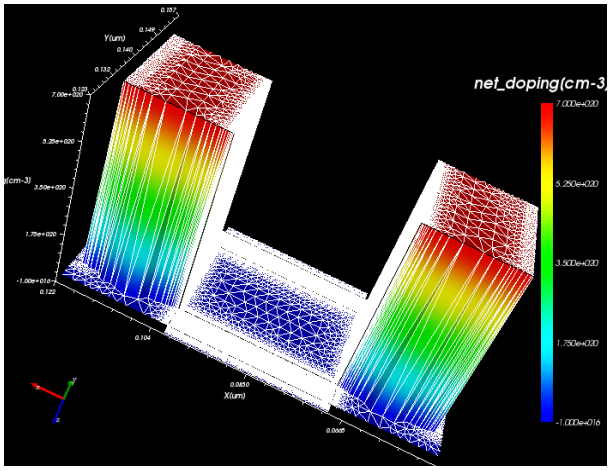

Fig. 4 3D View of Net doping for the device

Hence there is scaling restraint of double gate FinFETs that rely on gate-length and fin-thickness. Scaling limit is ratio of gate-length (L_g) to the fin width (W_{fin}). DIBL and sub threshold swing (SS) rises unexpectedly when the L_g/W_{fin} ratio drops below 1.5 [11].

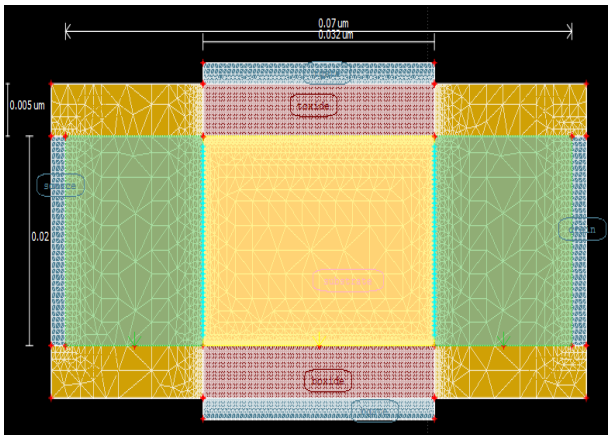

Fig. 5 Meshed FinFET

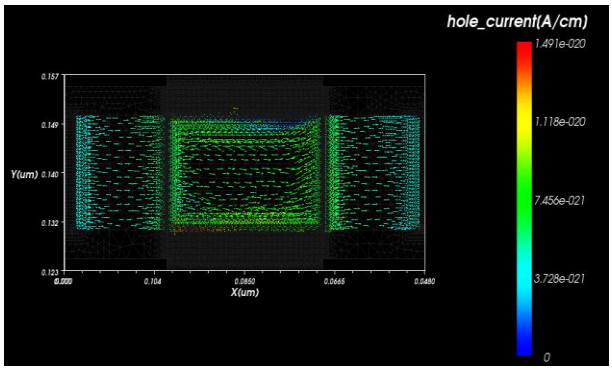

Fig. 6 Hole current at V_g=V_d=1.5V and I_d= 0.0410523mA

For gate length L_g =32 nm, determined scaling limit ratio for different fin widths of 5, 10, 20, 30, 40, and 50 nm are 6.4, 3.2, 1.6, 1.06, 0.8, and 0.6 respectively. Scaling ratio is above 1.5 for 5, 10, 20 nm fin width but for 30 nm it falls below 1.5. This shows that because of large DIBL and sub-threshold swing, in spite of having high drain current for 30, 40 and 50nm it is not advisable to fabricate the device above 22nm. At 32 nm gate-length and taking 1.5 as scaling limit we can calculate the maximum W_{fin} that can be fabricated is 21.33 nm. Scaling ratio is decisive factor that determines the short channel effects that further defines scaling capabilities. Expansion of fin width also leads to lower the threshold voltage of the device as gate to surface potential coupling rises with fin thickness [11]. The surface potential not only based on capacitive coupling between the gate and the channel region but also on the capacitance of source/fin and drain/fin junction for shorter channel lengths. Source/fin and drain/fin junction capacitances drops as depletion region of source/fin and drain/fin increases.

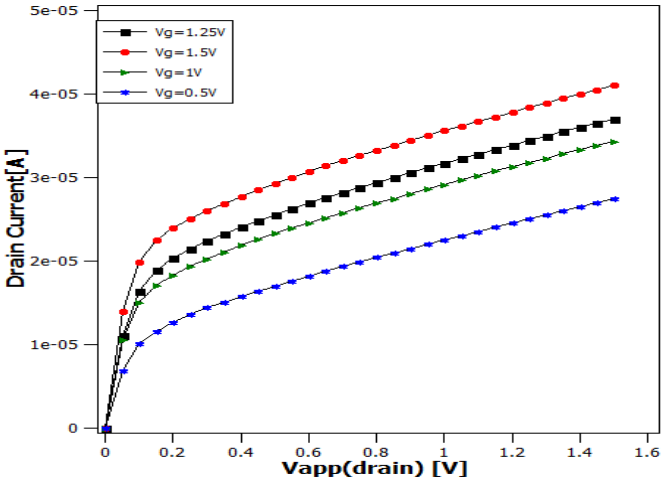

Fig. 7 I_d – V_d characteristics for 32nm gate length n-FinFET

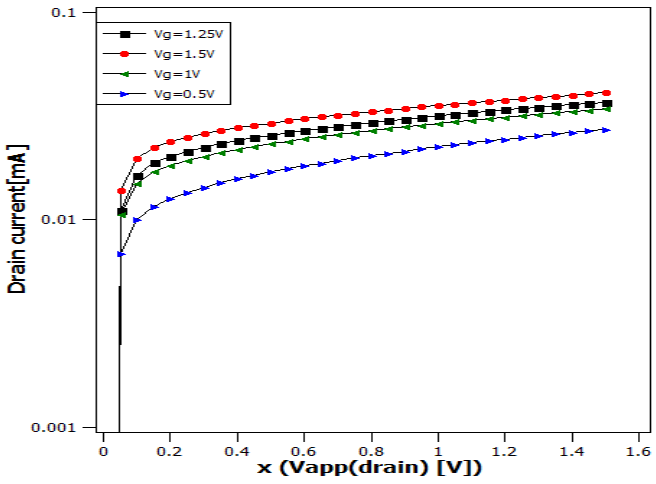

Fig. 8 I_d – V_d characteristics for 32nm gate length n-FinFET on logarithmic scale

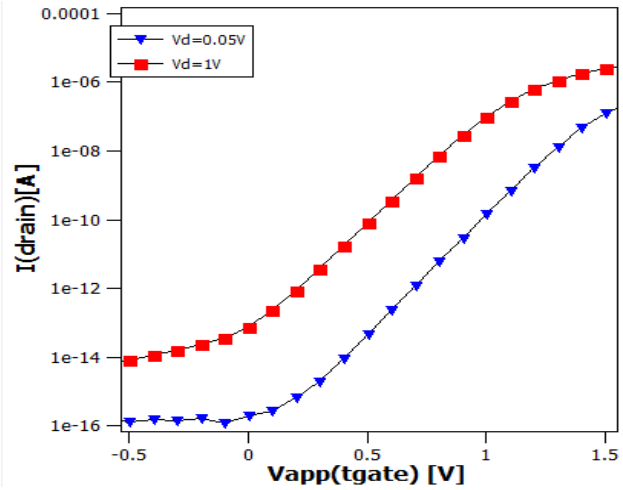

Fig. 9 Subthreshold I_d – V_g behavior (logarithmic scale) of 32nm gate length n-FinFET transistors

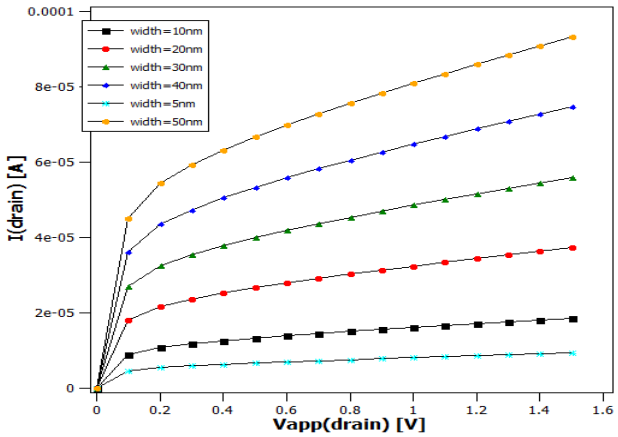

Fig. 10 IV characteristics in FinFET with fin thickness.

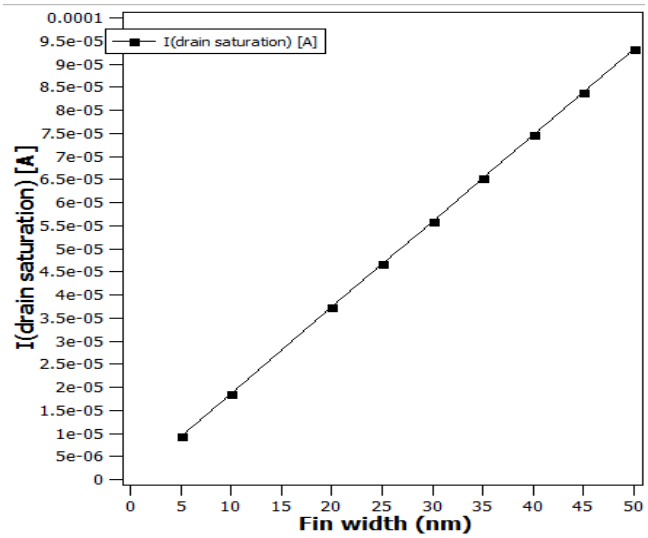

Fig. 11 Drain saturation current increases with fin thickness.

4. CONCLUSION

The steady state analysis of n-channel 32nm gate length FinFET at 22nm fin width has been done using visual 2D-TCAD software. As the supply voltage at gate is increased, there is rise in I_d which shows resistance reduces at higher V_g. The drain saturation current is 0.0343453mA at V_g=1V and 0.0410523mA at V_g=1.5V which indicates approximately 20% hike in I_d with increase in 0.5V gate voltage. Simulation of the FinFET device at distinct fin widths from 5 nm to 50 nm are demonstrated which shows that the slope of IV characteristic curve revamps with wider fins. For lean and confined dimension of fin a greater percentage of carriers are prone to scattering from sidewall which leads to the degradation with reducing fin width. And also thermal conductivity restraints at small fin width due to shortened phonon mean free path. Hence the device with wider fin width has valuable impact on drain current. But there is scaling limit of FinFET device which rely on scaling factor 1.5. For DG 32 nm FinFETs having width above 21.33 nm, the scaling ratio falls below 1.5. Hence in spite of having high drain current curves, there is large DIBL and sub threshold swing which consequences in short channel effects.

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