Communications on Applied Electronics (CAE) – ISSN : 2394-4714
Foundation of Computer Science FCS, New York, USA
Volume 3– No.3, October 2015 – www.caeaccess.org

Optimized Current-Mode Class-D RF Power Amplifier for Software Defined Radio

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ABSTRACT
This paper presents optimized Current-Mode Class-D (CMCD) RF Power Amplifiers (PA). The results demonstrate 73.63/79.75% Power Added Efficiency (PAE), for 29.5/26.5dBm output power in a standard 350/130nm CMOS technology at 2.4 GHz operation frequency for sine wave input. The proposed amplifier design is implemented using CADENCE tools (TSMC Foundry) and the simulation results are compared to the previous published work. Thank to intensive parameter optimization, the proposed design has succeeded in increasing the PAE.

Keywords
CMOS, Power Amplifier, CMCD, PAE, CADENCE

1. INTRODUCTION
Power amplifier is the most critical circuit in any wireless transmitter. The major bottleneck is found in achieving high power efficiency, which has a large impact in communication time and also in battery lifetime for portable wireless devices. Beside the high efficiency concern, modern mobile communication systems demand also cheap and reliable technologies. Submicron CMOS technology has already proved its feasibility for implementation of RF circuits beyond the GHz range [1, 2]. Moreover, due to the typical large scale density of CMOS circuits, the digital baseband and RF circuits can be both integrated on the same die, thus providing a low-cost and fully-integrated solution.

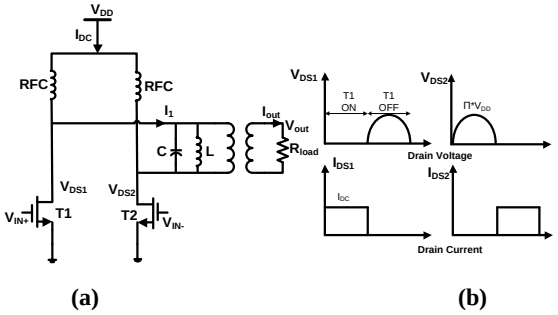
Ideally, switching amplifiers like class-D, E, and F can provide theoretically 100% efficiency because of non-overlapping drain voltage and drain current waveforms. But practically, their performance degrades due to parasitic capacitances and ON-resistance of the transistor switch. Current-Mode class-D (CMCD) power amplifiers similar to class-E power amplifiers, have an advantage that the drain capacitance of the output stage is absorbed into the output matching network. In addition, the output matching network for CMCD amplifiers is simple enough to be realized with few components. Thus, CMCD amplifiers can operate at higher frequency compared to other voltage mode switching amplifiers such as class-D amplifiers. So far, few class-D current mode amplifiers have been reported in CMOS technology [3, 4].

In this work, an intensive optimization approach for the design of a fully integrated CMOS CMCD PA is presented. The developed PA operates at a 5V/3V supply and delivers +29.5/+26.5dBm output power with 73.63%/79.75% PAE in a standard 350/130nm CMOS technology, respectively. The proposed PA can operate at 2.4 GHz and give high PAE at high output power compared to other published class-D PAs. Also, it has the largest 1dB bandwidth among the others.

The paper is organized such that section 2 contains the basic circuit of the amplifier and its operating principles. Section 3 introduces the amplifier design and the simulation results and the last section concludes the paper.

2. BASIC CIRCUIT AND OBERATION OF CMCD
For the interpretation of the real amplifier behavior, it is necessary to outline the ideal amplifier performance. Also, the practical amplifier is designed and operated to approach the performance of the ideal amplifier. Figure 1 shows the simplified schematic and ideal voltage and current waveforms of a Current-Mode class-D amplifier [5]. The CMCD amplifier is similar to the Voltage-Mode class-D amplifier with interchanged voltage and current waveforms. The current through the transistors is a square wave, while the voltage across the transistors is a half sine wave. The overlap of high voltage and high current is thus avoided to attain high efficiency and additionally, when the transistor turns ON, the voltage across the transistor is zero and so the output capacitance discharge problem is eliminated. A parallel LC resonator provides a short circuit for higher order harmonics and only the fundamental component reaches the load.

Figure 1(a) shows the CMCD circuit and Figure 1(b) shows the waveforms for each transistor. For the CMCD, current sources are used instead of voltage sources, and the two switching transistors control the current instead of the voltage. At the output between the two drains, there is a parallel-connected filter, with resonant frequency set to the carrier frequency. Due to the filter resonance, there is no voltage across the transistors at each switching instants and the so-called zero voltage ZVS is achieved. Even if the transistors have some output capacitance, the output capacitance can become part of the output parallel filter and consequently, the voltage waveforms remains as shown in Figure 1(b).This ZVS feature is a key advantage of the CMCD architecture. As mentioned above, another important switching condition, i.e., ZCS, avoids inductance losses by making the current zero at the instant of switching. VMCD and class-F achieve this condition. But, ZCS is less important than ZVS.



(a) **(b)**

Fig 1: CMCD circuits and waveforms.

However, for GHz-range applications, the VMCD amplifier has some drawbacks. The drain capacitance of the transistors are not a part of the matching network and need to be charged and discharged every cycle, leading to CV^2f power dissipation. Another disadvantage of the conventional Class-D PA is that it requires the use of a PMOS device, which has higher on-resistance than its NMOS counterpart. Typically, to achieve similar on-resistance as the NMOS switch, the PMOS switch size needs to be increased 2-3 times the size of the complementary NMOS , thereby increasing input capacitance significantly and making driver design more challenging.

The Current-Mode class-D amplifier has a constant biasing current I_{DC} flowing to the circuit through two current chokes. When T1 is off and T2 is on, half of the current I_{DC} goes through the filter circuit to T2. The other half flows directly to T2 through the other choke. The current I_1 flowing to the load network is a square wave with amplitude $I_{DC}/2$, By using Fourier series transform, the frequency components of the

load current can be express

$$I_1 = \frac{4I_{DC}}{2\pi}\left(\sin(\omega t) + \frac{1}{3}\sin(3\omega t) + \ldots\right) \quad (1)$$

Only the fundamental current flows through the primary winding of the balun, while the other frequency components pass through the parallel LC circuit. The first harmonic is then transformed to the secondary winding of the balun causing an output current I_{out}, where it flows through the load resistance R_{load} causing an output voltage V_{out}, that is given by

$$V_{out} = R_{load} I_{out} = \frac{2I_{DC} R_{load}}{\pi}\sin(\omega t) \quad (2)$$

In an ideal situation, the drain–source voltages V_{DS1}, and V_{DS2} are half-rectified sine waves and the drain currents I_{DS1}, and I_{DS2} are square waves. However, the drain source voltage DC value is V_{DD} which is equal to the average value of the half wave rectified drain to source voltage V_{DS}. Then by Fourier analysis it follows that:

$$V_{out,\max} = \pi V_{DD} \quad (3)$$

Then, by combining the above two equations, one can relate the DC current I_{DC} directly to V_{DD} and the load resistance R_{load} as:

$$I_{DC} = \frac{\pi^2}{2R_{load}} V_{DD} \quad (4)$$

The input power P_{in} and output power P_{out} of the Current-Mode Class-D amplifier is then given by,

$$P_{in} = P_{out} = V_{DD} I_{DC} = \frac{\pi^2}{2R_{load}} V_{DD}^2 \quad (5)$$

It is clear that the two powers are equal and so, the efficiency of the amplifier is 100%. In order to realize this efficiency, one would have ideal components operating at the prescribed waveform. It is the intension of every designer to approach these requirements.

In a real implementation at RF frequencies for the circuit of Figure 1, the current sources are replaced by a DC-feed inductor, as shown in Figure 2. The current-mode Class-D amplifier is the dual of a conventional class-D amplifier. However, the passive network complexity is greatly reduced in this topology. The parallel tank required in this design is realized using an on-chip transformer, which simultaneously performs impedance transformation and differential- to-single ended conversion. The architecture of transformer-coupled CMCD is thus very compact and amenable to integration in nano scale CMOS processes.

3. CMCD CIRCUIT DESIGN AND THE SIMULATION RESULTS

In this section, practical CMCD with maximized performance for software defined radio will be introduced. The practical Current-Mode class-D amplifier circuit is shown in Figure 2. To derive the differential output power transistors from a single ended source, an input balloon is used. The secondary of the balloon is connected to the gates of the NMOS transistors through coupling capacitors for DC isolation. The gates of the he transistors are biased by a DC voltage source V_b via an AC decoupling choke. The drains of the transistors are DC biased through two chokes working as a high impedance to inject constant currents in the drains of the transistor as required for the proper circuit operation. The output of the amplifier is differentially taken from the drain of the transistors across a parallel resonance circuit whose output voltage is connected to a single ended load by a balun.

The CMCD RF power amplifier is predesigned to work at a radio frequency of 2.4GHz. It is loaded by 50Ω load and driven by a source having impedance of 50Ω. The amplifier is powered by 5V at the drain and an adjustable bias voltage V_b at the gates. The coupling capacitors and the chokes values are selected to have the proper impedance level. The transistors are selected to have as small a possible on resistance while keeping their size as small as possible. The drain parasitic capacitances are added to the capacitor in the output tank.

After estimating the values of the circuit elements, their optimum values are found by circuit analysis using the integrated circuit design Software CADENCE to achieve the highest possible efficiency of the amplifier, assuming a sine wave input voltage. The final design values of the circuit elements are shown in the circuit diagram of Figure 2, with the two NMOS transistor widths of 1mm.

This circuit is analysed by CADENCE assuming 350 nm technology and typical voltage waveforms at the drain and at the output together with the input are shown in Figure 3. While the input voltage waveform is sine wave, the output voltage appears sinusoidal to great extent. The drain current shape should be a square wave non overlapping with the drain to source voltage pulses , but in reality it appear slightly overlapping the drain to source voltage waveform. The drain

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Volume 3– No.3, October 2015 – www.caeaccess.org

voltage waveform itself appears as a clamped sine waveform on the value of the power supply voltage.

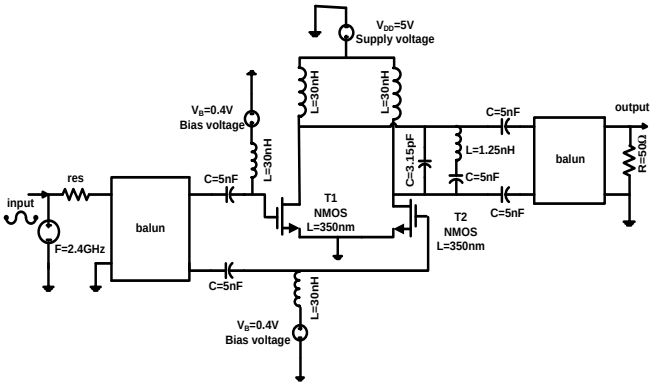

Fig 2: CMCD circuit for high frequency using 350nm technology

The optimum values of the circuit elements which are determined through simulation to get the maximum output power from the amplifier are included in Figure 2. As an outputs from the simulator, the DC current through the supply of 5V is 243mA and the DC dissipated power in the amplifier is $P_{DC}=I_{DC}\times V_{DD}$ = 1.215W. The current from the input sine wave signal is 6.5uA then the input power $P_i=I_i\times V_i$ = 0.012 mw Total consumed power from the input source and the supply voltage is then $P_{DS}=P_{DC}+P_i$=1.215W. To see where power is lost, the dissipated power in the T1 and T2 transistors are calculated and termed P_{T1} and P_{T2} respectively, while that delivered power to load resistor is termed $P_{RL.}$ They estimated to be P_{T1}= 160.2mW, P_{T2} =160.2mW and P_{RL} = 894.6mW.

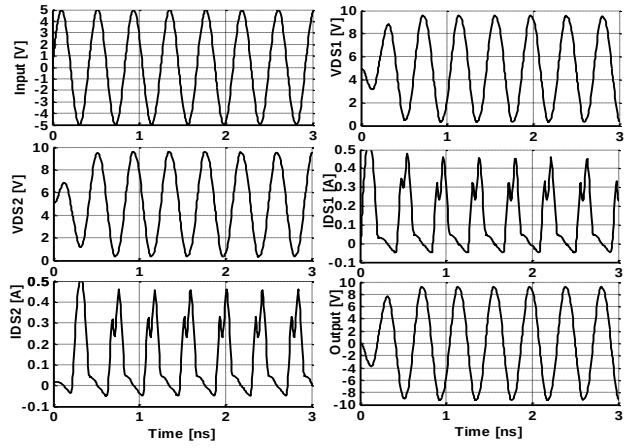

Fig 3: Current and voltage waveforms of the CMCD amplifier circuit for high frequency using 350nm technology

The total dissipated power in all the elements (PDE) = P_{T1} + P_{T2} + P_{RL}=1.215W, results in a Power Added Efficiency, PAE=73.63%. From the previous results it is seen that P_{DS} and P_{DE} are equal, which proves the power dissipation balance.

In order to see the effect of the transistor channel length on the amplifier performance parameters, we designed a similar amplifier circuit using 130 nm CMOS technology. The designed amplifier is depicted in Figure 4. Then we simulated the circuit and determined its major performance parameters.

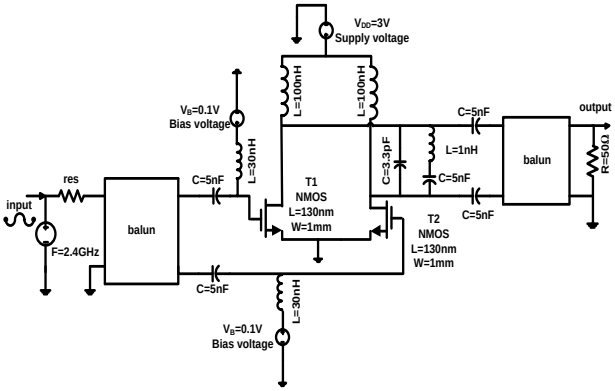

Fig 4: CMCD circuits for high frequency using 130nm technology

Calculation of power dissipation and drain efficiency for CMCD RF power amplifier based on 130nm CMOS technology shows that the DC current through the supply of 3V is 186.5mA, the DC dissipated power is $P_{DC}=I_{DC}\times V_{DD}$ = 559.5mW, the current from gate biasing voltage of 0.1v is 0.5uA leading to a negligible dissipated power from the gate biasing, and the current from the input sine wave signal is 4.8uA giving an AC input power $P_i=I_i\times V_i$ = 10uW. It follow that the total consumed power from the input source and the supply voltage $P_{DS}=P_{DC}+P_i$=559.5mW.

As has been done with the amplifier at 350 nanometre technology, to see where power is lost, the dissipated power in the T1 and T2 transistors are calculated and termed P_{T1} and P_{T2} respectively, and the delivered power to load resistor P_{RL} is determined. They estimated to be: P_{T1}= 56.6mW, P_{T2} =56.6mW and P_{RL} = 446.3mW.

The total dissipated power in all the elements PDE = P_{T1} + P_{T2} + P_{RL}=559.5mW, PAE is found to be about 79.75%. From the previous results the power balance is achieved such that P_{DS} and P_{DE} are equal, which proves the validity of the results.
Now the effect of the input source impedance variation on the amplifier efficiency is studied. Figure 5 shows that varying the source impedance from zero to 50 ohms has a remarkable effect on the PAE of the amplifier for both technologies. So, it is preferable to drive these amplifiers from a constant voltage source. However operating the amplifier with a source having an impedance up to 50 ohm may be acceptable. The best solution may be to build an on chip driver with very low source impedance. But this may be out of the scope of this paper.

To complete the characterization of the amplifiers, their frequency response is depicted in Figure 6 covering the frequency range from1.5 to 4 GHz. It is seen that the PA has a broad resonance peaks and a wide band width such that its one dB bandwidth amounts to 1.5 and 1.1 GHz, for 350nm/130nm technology, respectively.

Table 1 shows a comparison between CMCD PAs using 350nm and 130nm technology. The CMCD PA using 130nm technology has 6% improvement in the PAE at the expense of the output power where the shorter channel amplifier has a lower output power. However, the two technologies have appreciably high PAE, because CMCD power amplifiers are similar to class-E power amplifiers which have an advantage that the drain capacitance of the output stage is absorbed into the output matching network.

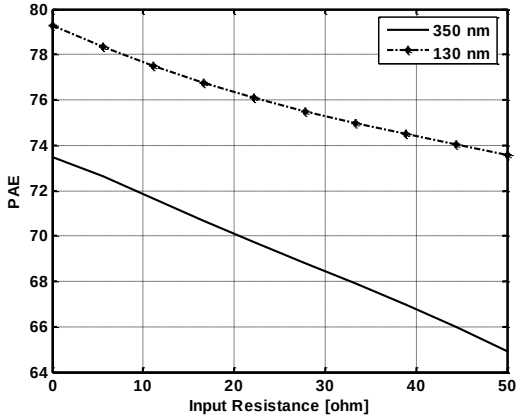

Fig 5: power added efficiency and output power versus source input resistance

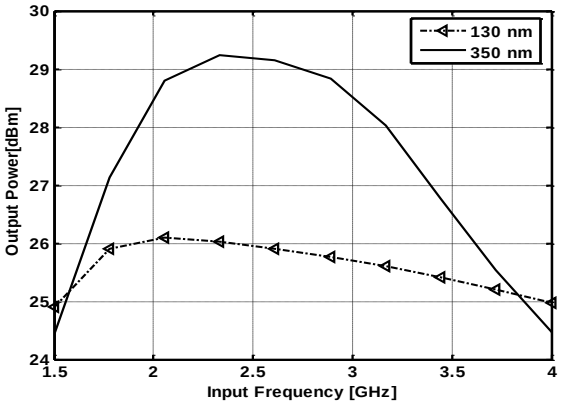

Fig 6: Output Power versus input frequency

Figure 7 shows the output power and PAE for the two technologies as a function of the power supply voltage, V_{DD}. As expected, the output power increases with V_{DD} while the PAE increases very slightly reaching a flat maximum and decreases again while the decrease of the 130 nm technology is much more pronounced than the 350 nm one.

Figure 8 shows the simulated PAE a function of the gate-bias voltage where the gate-bias voltage is swept from 0V to 2V. It is clear from this figure that there is a peak of the efficiency at specific gate bias voltage depending on the technology. The peak for the shorter channel lies at the zero gate bias and consequently, it is better to operate it at this voltage saving one power supply. As the gate bias increases from relatively low values, the ON-resistance of the transistor will decrease improving the efficiency until it reaches maximum value. After which, the resistance decreases again as the transistors can not be made OFF disrupting the class D operation.

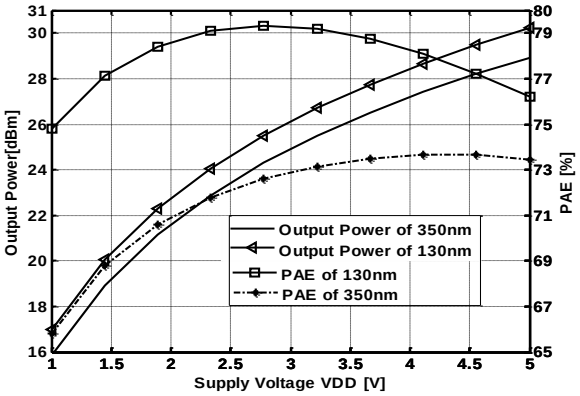

Fig 7: power added efficiency and output power versus supply voltage VDD

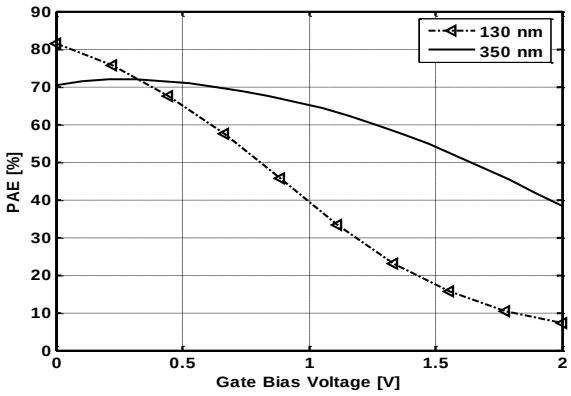

Fig 8: power added efficiency versus source gate bias voltage

For sake of comparison with the published results of class-D CMOS power amplifiers, Table 2 summarizes the performance parameters of the most recent publications. Recently, Broadband CMCD amplifier was demonstrated to attain an efficiency of 45% at RF frequency of 1.8 GHz with an output power of 26.8 dBm using 130 nm CMOS process and encapsulated in QFN package [6]. In [4], a CMCD power amplifier has been designed in 90-nm technology, achieving 76% maximum drain efficiency, with 16-dBm of output power at 2.45-GHz, using solely on-chip components. In [7] a VMCD RF PA operating at frequency of 1.85GHz, and supply voltage of 5.5V delivers +32 dBm in a standard 130nm CMOS technology this voltage mode PA utilizes four on-chip transformers to combine the outputs of eight Class-D stages. Our PA presented in this work operates at 2.4GHz and gives a best trade-off between PAE and output power with respect to the other published class-D PAs, The proposed power amplifier has largest1dB bandwidth among the tabulated amplifiers.

Table 1. Performance summary of CMCD Class-D PA

Technology	F [GHz]	V_{DD} [V]	Pout [mW]	P_D [mW]	Pout [dBm]	PAE [%]
350nm	2.4	5	894.6	1215	29.5	73.63
130nm	2.4	3	446	559.5	26.5	79.75

Table 2. Comparison of Class-D CMOS RF PAs-Peak Values

Ref.	Year	Mode	*Pout* [dBm]	V_{DD} [V]	PAE [%]	*F* [GHz]	Tech [nm]	BW [GHz]
[8]	2012	CMCD	21.8	1	44	2.25	65	0.8a
[9]	2013	VMCD	29.7	5.5	26.6	1.95	65	1.6b
[4]	2009	CMCD	16	1	76	2.45	90	-
[7]	2011	VMCD	32	5.5	15.3	1.85	130	0.9b
[6]	2014	CMCD	26.8	2.4	45	1.8	130	-
This work		CMCD	29.5	5	73.63	2.4	350	1.5a
			26.5	3	79.75	2.4	130	1.1a

(a) 1 dB and (b) 3 dB bandwidth (BW)

4. CONCLUSION

This paper presented the optimized design and the simulation for the current-mode class-D RF PA which can operate at a 5V/3V supply and deliver +29.5/+26.5 dBm with 73.63% /79.75% PAE at an operating frequency of 2.4GHz, in a standard 350/130nm CMOS technology. The comparison with the recently published amplifiers showed that the performance parameters of the developed amplifiers outperform many previous deigns thank to very intensive parameters optimization. It remains that these amplifiers be fabricated to get out its final operational characteristics. In order to avoid the losses in the integrated coils one may use a bond wire inductors.

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