*Communications on Applied Electronics (CAE) – ISSN : 2394-4714*
*Foundation of Computer Science FCS, New York, USA*
*Volume 3– No.7, December 2015 – www.caeaccess.org*

# Modified PFAL Adiabatic Technique for Low Power

Bhakti Patel
M.E. Student
EXTC Department
Mumbai University.

Poonam Kadam
Assistant Professor
EXTC Department
Mumbai University.

## ABSTRACT
This paper presents the quasi-adiabatic Modified Positive Feedback Adiabatic Logic (MPFAL) for low power operation through energy recovery technique. The circuit of positive feedback adiabatic (PFAL) inverter has been improved here. It is a diode-free and dual rail logic offering both the true and complementary outputs. Validation is done through basic digital gate circuits. Comparison with static CMOS and PFAL circuits are made to prove the designs. In post-layout simulations, energy savings of 27% is achieved against the optimized PFAL Inverter, NAND and NOR gate circuits. The various improvement results are analyzed in LTSPICE tool.

## General Terms
Power dissipation, VLSI, adiabatic logic

## Keywords
Static CMOS, PFAL, NAND, NOR

## 1. INTRODUCTION
In the past, the major concerns were area, cost and performance. Power is the secondary concern. But now a day, power is the main concern due to more use of handheld personal computing devices. For high performance portable device such as laptop, the goal is to reduce the power dissipation of the electronics portion of the system to a point which is half of total power dissipation [1].

The power dissipation in conventional CMOS design circuits can be minimized by reducing the supply voltage value and switching activity. But reducing the values of these parameters may degrade the performance of the device [2]. So an efficient low power technique such as adiabatic technique is needed that has less power dissipation compared to CMOS. This technique is based on adiabatic logic principle. Adiabatic logic is reuse the energy stored in the load capacitors rather than the discharging the load capacitors to the ground and wasting this energy.

In this paper two technique PFAL and Modified PFAL are analyzed using basic logic gates like NAND, NOR and inverter circuits. LTSPICE [3] software is used for circuit implementation and simulation with standard CMOS technology parameters.

The paper is organized as follows: Section II introduced the conventional CMOS inverter Design. Section III follows the introduction with the operation of PFAL inverter and modified inverter circuits and its performance. Section IV presents the results and compares them with the CMOS and PFAL circuit counterparts. Section VI concludes.

## 2. ADIABATIC LOGIC DESIGN

### 2.1 PFAL

#### *2.1.1 PFAL Inverter*
PFAL which is stands for Positive Feedback Adiabatic Logic was introduced by A.Vetali in 1996 [4]. It uses dual rail logic implementation strategy. It consists of cross-coupled inverter stages maintaining the two output terminals with two complementary inputs function (*F*) and complement-function (*F*bar) at both the end. The logic blocks are implemented with NMOS transistors only [5]. The logic function in the functional block can be realized with only NMOS transistors connected to parallel PMOS transistors here. PFAL inverter simulation is shown in below figure 1.

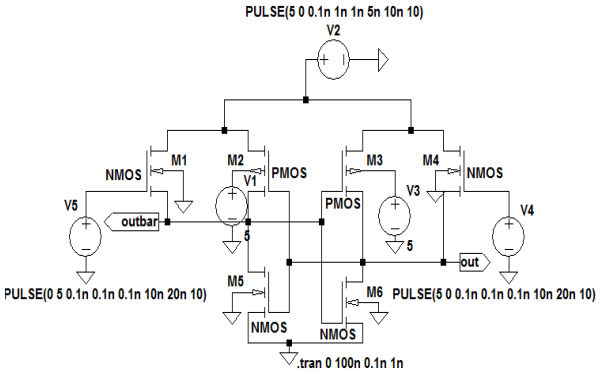


**Fig. 1: Basic Structure of PFAL Inverter**

During evaluate phase of clock, in is high and in bar is low. Also one of the two NMOS (M1 at inside, M4 at in bar side) from N-functional block, M1 is on. Out follows raising edge of power clock by charging nodal capacitance Cout. At this time, M1 remains off because in bar signal is low. Now because of high out at its gate, M3 conducts to pull low out bar. This results in charging of Out node as M2 was pushed ON. Now M1 is off and M3 is on due to high Out at their gate terminal. Also M4 is off due to low Out bar at its gate terminal.

During hold phase, in starts falling and M4 continues its conduction until clock is more than threshold voltage of PMOS, beyond its stops conductions.

During recovery phase, recovery occurs through M2 PMOS transistor. Then, conduction happens through M2 and M4. Now, when in bar is high, M4 conducts providing ground to out. This avoids floating output problem [6].

The transient simulation results are as shown in the Figure 2

*Communications on Applied Electronics (CAE) – ISSN : 2394-4714*
*Foundation of Computer Science FCS, New York, USA*
*Volume 3– No.7, December 2015 – www.caeaccess.org*

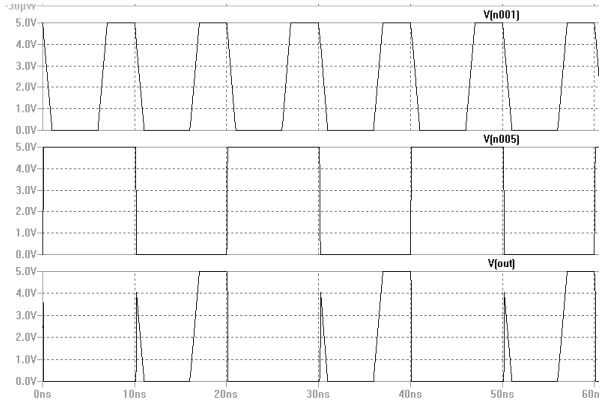


**Fig. 2: Voltage waveform of PFAL inverter**

Fig. 2 shows the simulated waveforms of PFAL inverter, where the uppermost signal indicate power clock, after that input signal and the bottom signal is output signal.

### *2.1.2 PFAL NAND Gate*

The partially adiabatic PFAL with two-input NAND gate can be implemented as shown below in the Figure 3 using standard LTSpice Tool technology and simulated waveforms is shown in Figure 4, respectively.

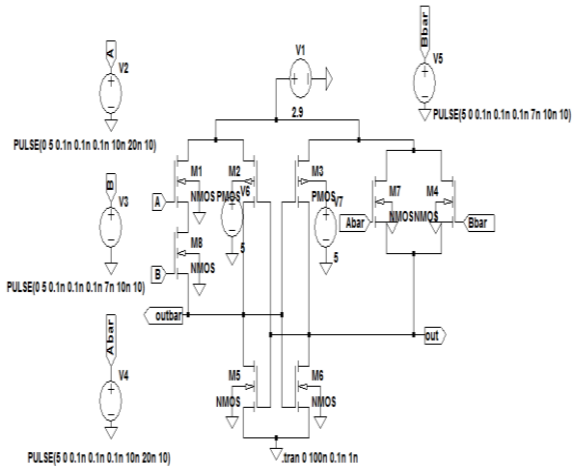


**Fig 3: Basic Structure of PFAL NAND Logic Gate**

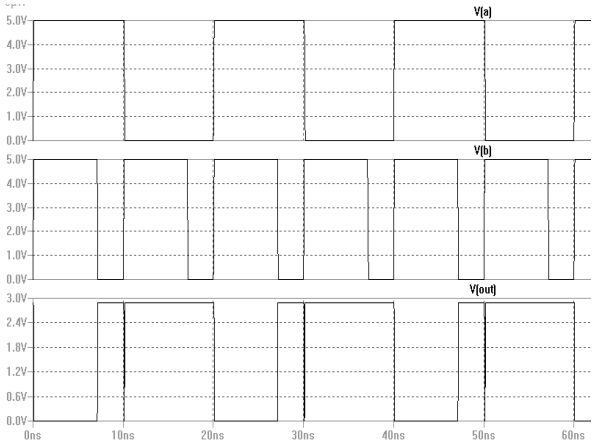


**Fig 4: Voltage waveform of PFAL NAND Logic Gate**

Fig. 4 shows the simulated waveforms of PFAL NAND, where the uppermost signals indicate input signals and the bottom signal is output signal.

### *2.1.3 PFAL NOR Gate*

The partially adiabatic PFAL with two-input NOR gate can be implemented as shown below in the Figure 5 using standard LTSpice Tool technology and simulated waveforms is shown in Figure 6, respectively.

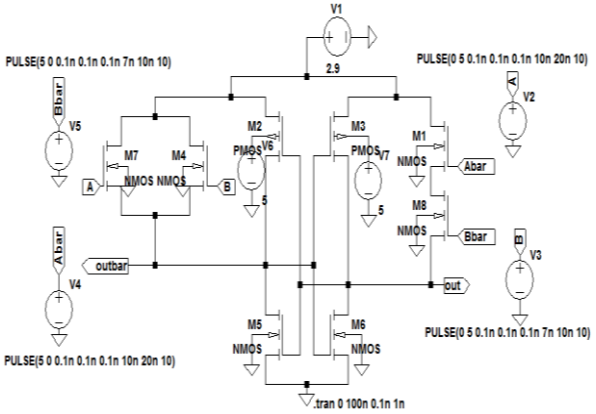


**Fig 5: Basic Structure of PFAL NOR Logic Gate**

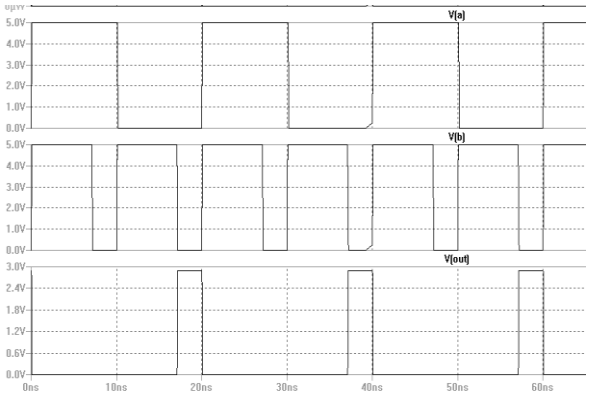


**Fig 6: Voltage waveform of PFAL NOR Logic Gate**

Fig. 6 shows the simulated waveforms of PFAL NOR, where the uppermost signals indicate input signals and the bottom signal is output signal.

## 2.2 Modified PFAL

### *2.2.1 Modified PFAL Inverter*

The circuit diagram for modified PFAL adiabatic circuit is shown in Figure 7. It implements basic Inverter functionality. It uses an additional drain gate connected NMOS transistor, in between the source and ground terminal of PFAL cross-coupled inverters to reduce the power dissipation more than PFAL inverter design [7].

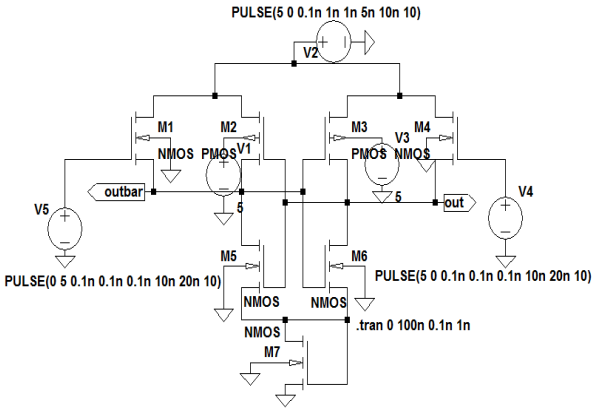


**Fig 7: Basic Structure of MPFAL Inverter**

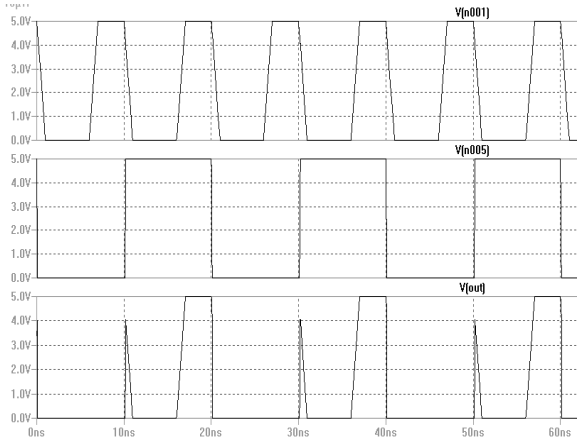


**Fig 8: Voltage waveform of MPFAL inverter**

Fig. 8 shows the simulated waveforms of MPFAL inverter, where the uppermost signal indicate clock signal, after that input signal and the bottom signal is output signal.

## *2.2.2 Modified PFAL NAND Gate*

The partially adiabatic PFAL with two-input NAND gate can be implemented as shown below in the Figure 9 using standard LTSpice Tool technology and simulated waveforms is shown in Figure 10, respectively.

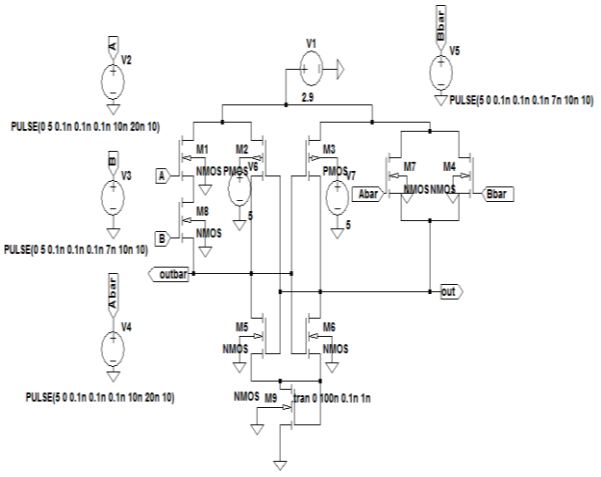


**Fig. 9: Basic Structure of MPFAL NAND Logic Gate**

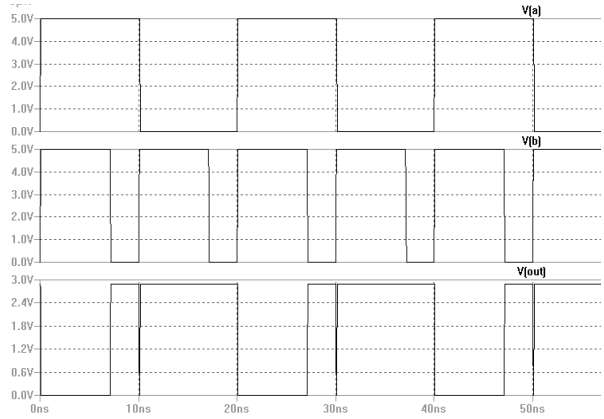


**Fig. 10: Voltage waveform of MPFAL NAND Logic Gate**

Fig. 10 shows the simulated waveforms of MPFAL NAND, where the uppermost signals indicate input signals and the bottom signal is output signal.

## *2.2.3 Modified PFAL NOR Gate*

The partially adiabatic PFAL with two-input NOR gate can be implemented as shown below in the Figure 11 using standard LTSpice Tool technology and simulated waveforms is shown in Figure 12, respectively.

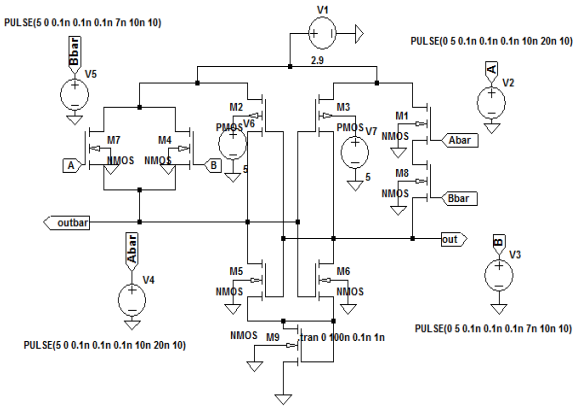


**Fig. 11: Basic Structure of MPFAL NOR Logic Gate**

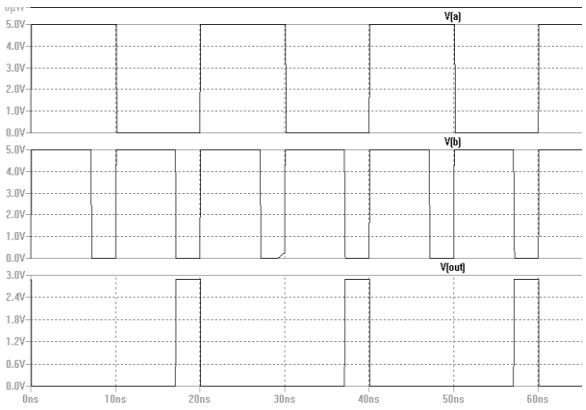


**Fig. 12: Voltage waveform of MPFAL NOR Logic Gate**

Fig. 12 shows the simulated waveforms of MPFAL NOR, where the uppermost signals indicate input signals and the bottom signal is output signal.

## 3. RESULTS AND DISCUSSION

This section showed the comparison of the conventional CMOS logic style with the low power adiabatic logic style. Table I, II& III indicate the power comparison made for the proposed inverter, NAND and NOR gates constructed using PFAL and MPFAL adiabatic structures. The analysis is made for various voltages across a range of 4V to 5V, to validate the design.

**Table 1. Power Comparison at Different Voltages**

| Inverter Type | Power consumption in watts | | |
|---|---|---|---|
| | **4v** | **4.5v** | **5v** |
| CMOS Inverter | 895.14m | 1.074m | 1.223m |
| PFAL Inverter | 180.30u | 245.52u | 324.63u |
| MPFAL Inverter | 77.37u | 107.31u | 132.52u |

**Table 2. Power Comparison at Different Voltages**

| | Power consumption in micro watts | | |
|---|---|---|---|
| | **4v** | **4.5v** | **5v** |
| CMOS NAND Gate | 225.28 | 267.17 | 341.43 |
| PFAL NAND Gate | 208.96 | 260.06 | 321.19 |
| MPFAL NAND Gate | 75.73 | 102.14 | 122.52 |

**Table 3. Power Comparison at Different Voltages**

| | Power consumption in micro watts | | |
|---|---|---|---|
| | **4v** | **4.5v** | **5v** |
| CMOS NOR Gate | 158.42 | 196.14 | 235.63 |
| PFAL NOR Gate | 115.51 | 160.60 | 212.84 |
| MPFAL NOR Gate | 47.95 | 80.39 | 103.24 |

In Table III shows the transistor count in various adiabatic architecture for inverter and NAND gate in comparison with CMOS inverter and NAND gate. It is found that our proposed adiabatic logic families uses more transistor count than compared to CMOS. In spite of using more transistor count than CMOS there is significant reduction in power consumption as compared to CMOS implementation.

**Table 4. Transistor Count Comparison of Various Circuits**

| | Number of Transistors | | |
|---|---|---|---|
| | **CMOS** | **PFAL** | **MPFAL** |
| Inverter | 2 | 6 | 7 |
| NAND Gate | 4 | 8 | 9 |
| NOR Gate | 4 | 8 | 9 |

## 4. CONLUSION

From the simulation results we analyzed the power consumption of various circuits shown in above Table 1, 2, 3. Results clarified that modified PFAL inverter has better performance than the normal PFAL inverter. The modified PFAL inverter has 70% less power dissipation over PFAL inverter. The modified PFAL universal gate (NOR) has 30% less power dissipation over normal PFAL circuits. The analysis shows that designs based on adiabatic principle gives superior performance when compared to conventional CMOS in terms of power even though their transistor count is high in some circuits.

## 5. FUTURE SCOPE

Study of modified positive adiabatic logic connected with multiplexers, multipliers and different types of adders in different parameters will be measure. Area efficient layout design analysis of shifter and rotator will be formed using MPFAL logic. Also measure dissipated energy at higher frequencies.

## 6. REFERENCES

[1] Arun Kumar, Manoj Sharma, Design and analysis of MUX using adiabatic techniques ECRL and PFAL, IEEE , 2013.

[2] G. Sujatha, Dilli kumar, "design of 2x2 bit cube in different low power Techniques for portable devices", International Journal of Advances in Science Engineering and Technology, ISSN: 2321-900, Volume-1, Issue- 2, Oct-2013.

[3] LTspice/SwitcherCAD III, Version 2.24i, US Pacific.

[4] A. Vetuli, S. Di Pascoli, and L.M. Reyneri, "Positive feedback in adiabatic logic", Electron.Lett, Vol.32, Sept. 1996.

[5] A. Blotti, S. Di Pascoli and R, Saletti, Sim le model for positive-feedback estimation adiabatic logic, Electronics letters, 20th January 2000, Vol. 36 No. 2.

[6] Bhakti Patel, Poonam Kadam, "Comparative Analysis of Adiabatic Logic Techniques",IJCA,Sept.2015

[7] Manoj Sharma and Arti Noor," Reconfigurable CPLAG and Modified PFAL Adiabatic Logic Circuits", Advanced Electronics, Vol.2015

[8] Ashmeet Kaur Bakshi, Manoj Sharma, Design of Basic Gates using ECRL and PFAL, IEEE, 2013.

[9] B. Dilli Kumar, M. Bharathi, Design of Energy Efficient Arithmetic Circuits Using Charge Recovery Adiabatic Logic, International Journal of Engineering Trends and Technology- Volume 4, Issue1- 2013.

[10] Renuka Verma, Rajesh Mehra, Area Efficient Layout Design Analysis of CMOS Barrrel Shifter, EATHD-2015 Conference Proceeding, 14-15 March, 2015.