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Synthesis of Peres and R Logic Circuits in Nanoscopic Scale

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ABSTRACT
Traditional lithography based VLSI architecture expanded to optimize higher scale integration and low powered computing of semiconductor components. This tend encounter severe challenges of short channel issue, tunneling and variation of doping. Quantum Dot Cellular Automata (QCA) is an esteemed nano-scale technology and a better substitute of Complementary Metal Oxide Semiconductor (CMOS) for it's transformation technique and computation method. Information-lossless or reversible logic circuits has divers precise utilization in communications, digital signal processing (DSP), computer graphics also in quantum computation. This paper presents the systematic model of Peres gate (PG) and R gate in QCA and CMOS. To simulate and verify the proposed design QCADesigner and Microwindlite, widely used simulation tools are used. Those proposed design has a promising future and can be used in modeling complex computing structure and nano-scale based low power consumption information processing structure.

Keywords
QCA, Peres gate, R gate, QCADesigner, MICROWIND.

1. INTRODUCTION
Nanotech has been the focus of a comprehensive analysis to repudiate the limitations of CMOS and imparts a unique magnitude for computing. Today it is admitted that next two decades, semiconductor production will have to preface applying new nanoelectronic materials [1]. Quantum dot Cellular Automata is a favorable technology for forthcoming ICs [2, 3] and a better substitute of complementary metal oxide semiconductor (CMOS) technology [4]. The reversible circuits compose the decisive architecture of quantum computers and typically used in power deprecation having the influence in emerging technologies as low power CMOS design, quantum computing, computer graphics, cryptography, communication, and optical computing [5, 6, 7, 8]. In the early 1960s, R. Landauer manifested that high technology circuits and systems constructed using irreversible logic circuit outcomes in energy dissipation due to information slump. Landauer's principle demonstrates that the loss of one bit of information lost, will depletes $kTln(2)$ joules of energy, where k is the Boltzmann's constant and T is performing temperature in Kelvin [9]. Later Bennett reveals that a zero power dissipation in logic circuits is conceivable, if it is contrived of reversible circuits [10]. Reversible circuits can be viewed as exclusive instance of quantum circuits as quantum expansion must be reversible [11]. In the area of quantum computing there are divers propositions on reversible circuit design like Feynman Gate [12], Toffili Gate [13], Fredkin Gate [14], NFT Gate [15] but very less of them are designed in a competent means in QCA [16, 17, 18]. The paper presents the architecture of Peres gate (PG) and R gate in QCA which is effectual than earlier designs and also presents the CMOS design of each individual layout.

2. BASICS OF QCA
The basic building segment of QCA is QCA cell and the cell is composed of four quantum dots located at the edges of the squared cell and two loose electrons. Depending on the location of the electrons, QCA cell has two form of polarization [19, 20]. The polarization of electrons are defined as P= +1 for logic '1' and P= -1 for logic '0' shown in figure 1.

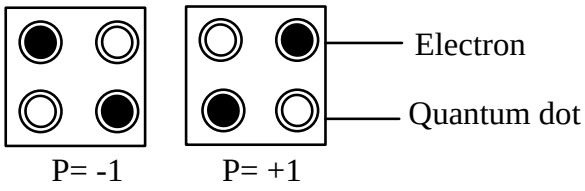
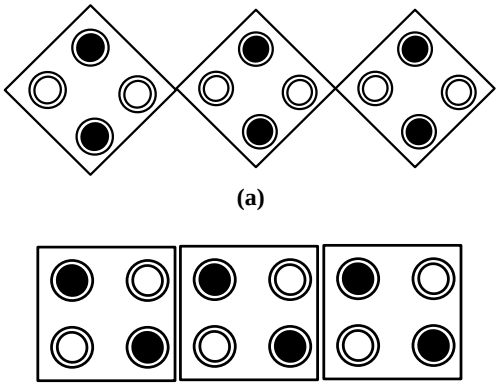


Fig 1: Basic structure of a QCA cell

The elemental entity of QCA based layout is QCA wire, majority gate and inverter [20]. QCA wire is a cluster of cells which regulated one by one and the polarization of each cell is explicitly influenced by the polarization of its neighboring cells accordingly electrostatic force. QCA wires can be either contrived up of 45^o cells or 90^o cells shown in figure 2. Basically QCA wires used to proliferate binary data from one end to another.



(a)

(b)

Fig 2: QCA wire (a) 45^o (b) 90^o

Roughly a majority voter composed of five cells and three of them are inputs, one output and one is middle cell. The center cell named device cell by reason of its action, switches to primary polarization [20]. Majority Voter can be expressed as MV (A, B, C) = AB + BC + AC. Using majority gate two primitive gates "AND" and "OR" can be implemented by assign one of the input fixed to 1 or 0 value. Figure 3 shows when C=1 the output is A+B which means OR function and when C=0 the output is AB that indicates the AND function.

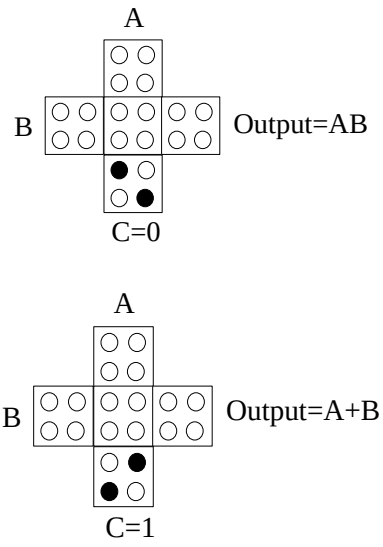


Fig 3: Majority Voter as AND gate (C=0) and OR gate (C=1)

QCA inverter returns the reverse value of input. This inverter is built of four QCA wires or seven cell. The input polarization is slit into two polarizations and finally, two wires join and make the opposite polarization shown in figure 4.

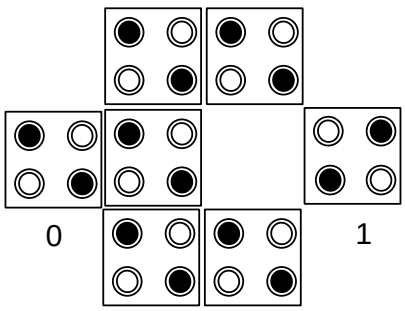


Fig 4: QCA seven cell inverter

3. PROPOSED CIRCUIT AND PRESENTATION

A circuit is called reversible if there is a one to one correspondence between its input and output positions or a gate is called reversible if the function it computes is bijective. A reversible circuit should be formed using nominal number of reversible gates. This section presents the proposed structures of Peres and R gate.

3.1 Peres Gate

Peres gate (PG) is a 3-input, 3-output, reversible gate [21] where the input is I (A, B, C) and corresponding output is O (P, Q, R). The outputs are defined by P=A, Q=A⊕B and R=AB⊕C. The quantum cost of Peres gate is 4. Figure 5(a) presents the block diagram of Peres gate and (b) shows the QCA representation.

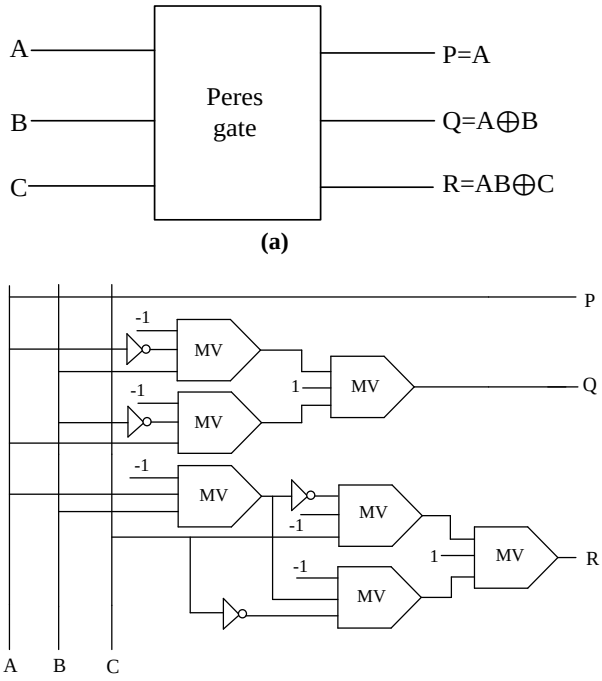


Fig 5: Block diagram of (a) Peres gate (b) proposed diagram of Peres gate in QCA

Table 1. Truth table presentation of peres gate

Input			Output		
A	**B**	**C**	**P**	**Q**	**R**
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

3.2 R Gate

The R gate is a 3x3 reversible gate [22]. Figure 6 shows the block diagram and QCA diagram of R gate. The input vector defined as I (L, M, N) and the output vector is O (X, Y, Z). The outputs are followed by X=L⊕M; Y=L and Z=LM⊕N'.

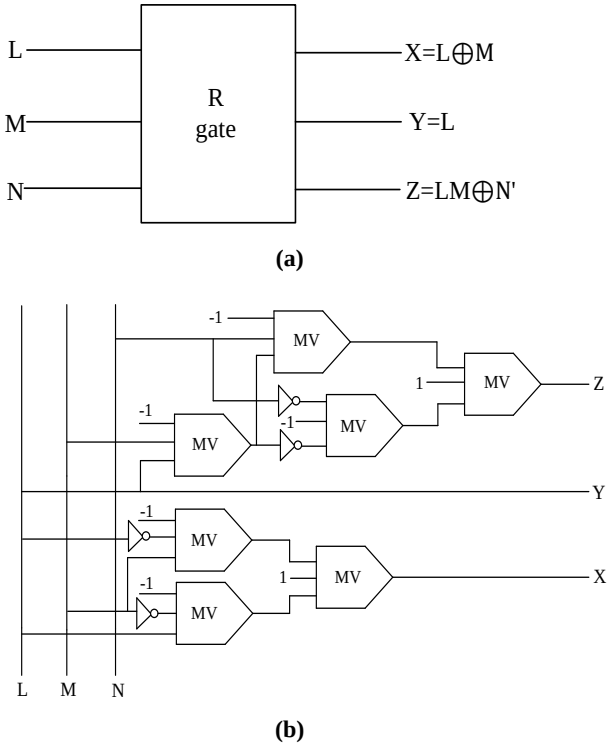


Fig 6: Block diagram of (a) R gate (b) proposed diagram of R gate in QCA

Table 2. Truth table presentation of R gate

Input			Output		
L	**M**	**N**	**X**	**Y**	**Z**
0	0	0	0	0	1
0	0	1	0	0	0
0	1	0	1	0	1
0	1	1	1	0	0
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	0	1	0
1	1	1	0	1	1

4. TECHNICAL IMPLEMENTATION OF PERES AND R CIRCUIT

Various proximate simulators such as the bistable simulation and nonlinear approximation are employed for testing the design level. But these approaches are iterative so it cannot produce the certain products. Finally QCA Designer ver. 2.0.3 is picked and this simulation engine is explained [23]. The definiteness of the proposed circuits are estimated by the simulation tool of QCA Designer ver. 2.0.3 [24]. The technical presentation are shown below.

4.1 Peres Gate

The quantum implementation of peres circuit has been urged by various authors [25] which is shown in figure 7(a) and figure 7(b) delineates the proposed peres circuit

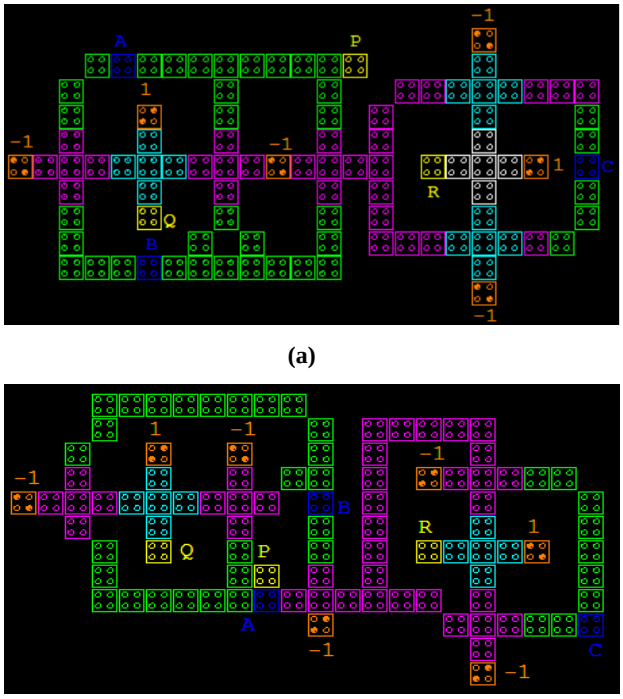


Fig 7: QCA simulated circuit design of (a) Peres circuit (b) proposed Peres circuit

4.2 R Gate

The QCA implementation of R circuit is shown in figure 8(a) and has been proposed by distinct authors [26]. The proposed R circuit is shown in Figure 8(b).

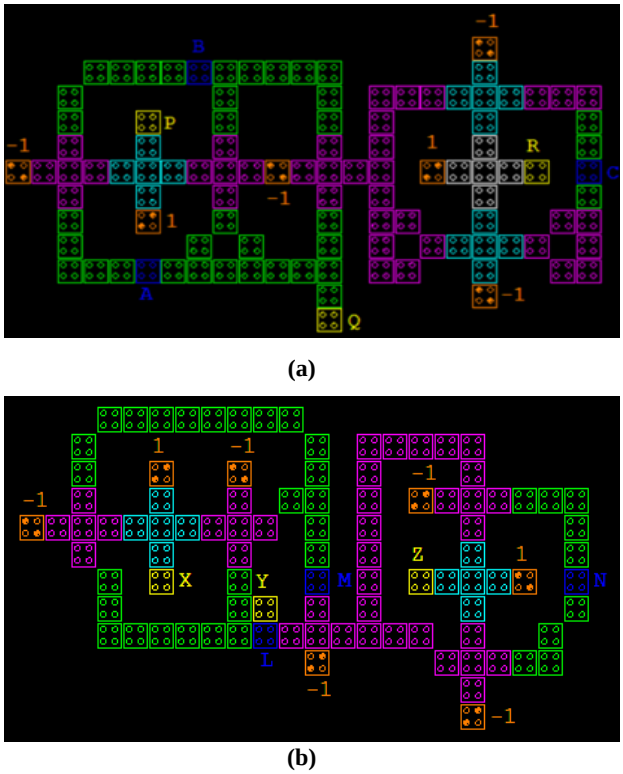
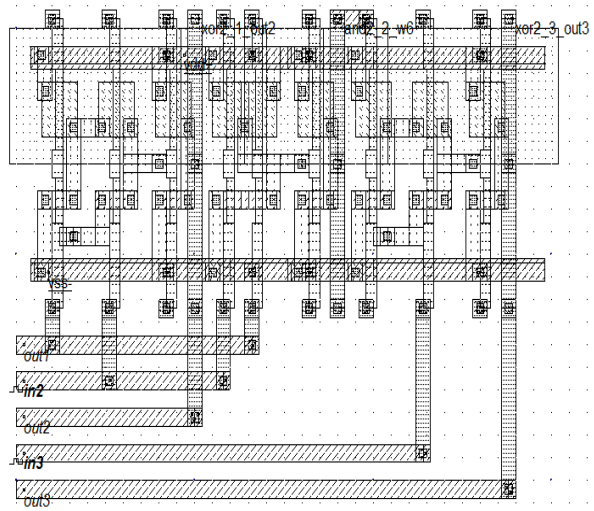


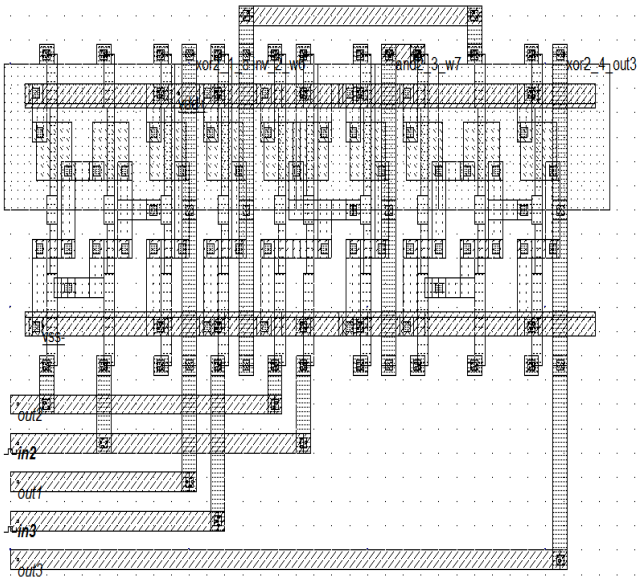
Fig 8: QCA simulated circuit design of (a) R circuit (b) proposed R circuit

Clock zones

For simulation and composition the proposed circuits in CMOS, MICROWIND [27] a PC tool for CMOS design is employed. This engine is very user-friendly to model and find out the covered space of any logic circuit as shown in figure 9 where (a) prescribed the peres circuit and (b) specify the R circuit.



(a)



(b)

Fig 9: Simulated circuit design of (a) Peres gate (b) R gate

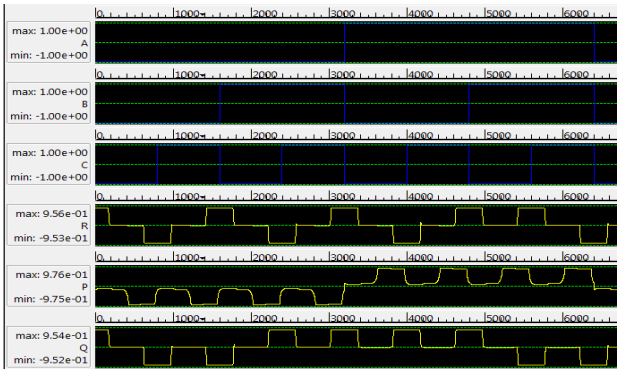
5. SIMULATION AND RESULT ANALYSIS

The urged logic circuits were functionally simulated using QCA Designer ver. 2.0.3. The successive criterions of the bistable approximation and coherence vector is used which are the default rates in QCADesigner. These parameters are shown in table 3.

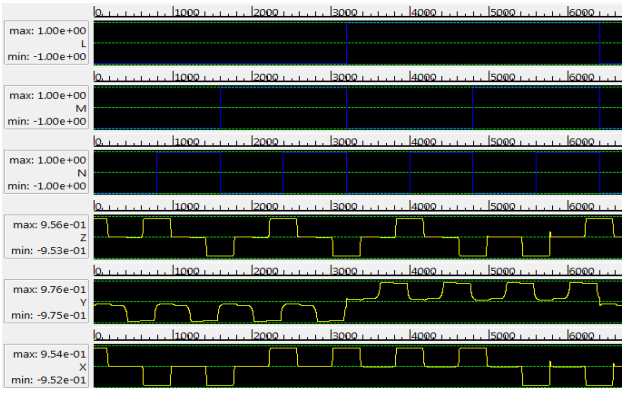
Table 3. Criterions of Bistable Approximation and Coherence Vector

cell size	18nm
dot diameter	5.000
number of samples	12800
relaxation time	1.000000e–15s
radius of effect	65.000000nm
time step	1.000000e–16s
convergence tolerance	0.001000
relative permittivity	12.900000
clock shift	0
clock amplitude factor	2.000000
layer separation	11.500000
clock high	9.800000e–022 J
clock low	3.800000e–023 J
upper threshold [1]	0.500
lower threshold [0]	-0.500
total simulation time	7.000000e–11 s
maximum iterations per sample	100

The simulated outcomes of the proposed circuits are shown below.



(a)



(b)

Fig 10: Simulated results in QCADesigner (a) Peres circuit (b) R circuit

Table 4. Performance Analysis of Proposed Circuits

Criterion	Peres circuit	Proposed Peres circuit	R circuit	Proposed R circuit
Cell number	99	96	105	96
Clock delay (Clock cycle)	1.00	0.75	0.75	0.50
Area in QCA (μm^2)	0.1008	0.105	0.126	0.109
Area in CMOS (μm^2)	59.8		71.4	
Improvement (in times)	570		655	

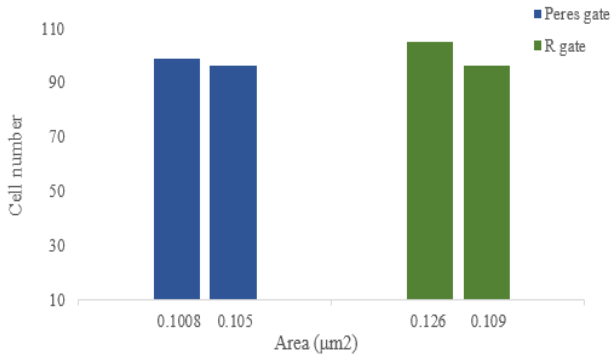


Fig 11: Comparative figures for cell and area of proposed Peres and R circuit

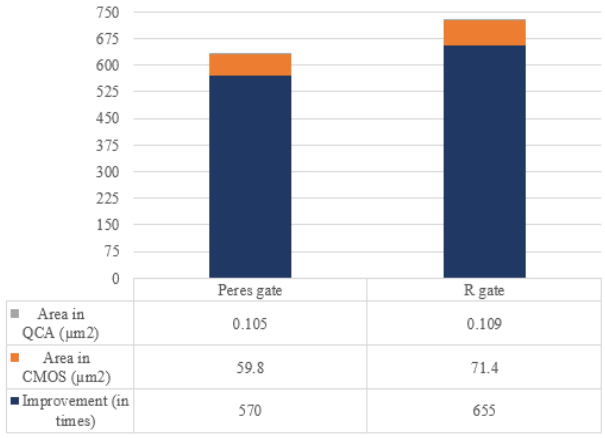


Fig 12: Comparative figures for area of QCA and CMOS with improvement

6. CONCLUSION

This paper analyzes an innovative design of Peres and R circuit and approved in terms of area and cell complication. Also the design of QCA based circuits with smaller feature size and ultralow power consumption than typical CMOS have been conferred in this paper. The simulation sequel show that the proposed design perform well. Hence, it consummates that the urged layout could be an auspicious step for future computing like quantum computers and ultralow power design in nanotechnology.

The forthcoming work can be extended as to design systems to handle larger and more general circuits with the inevitable objective of synthesizing quantum circuits.

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