Communications on Applied Electronics (CAE) – ISSN : 2394-4714
Foundation of Computer Science FCS, New York, USA
Volume 4– No.4, February 2016 – www.caeaccess.org

Design of a Sensitive Low Noise Amplifier for Wireless Communication

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ABSTRACT
The Sensitivity of a Low Noise Amplifier (LNA) plays a very important role in wireless Communication. The Radio Frequency (RF) and Low Noise Amplifier (LNA) is essential in amplifying required high frequency RF signal without distortions and other impairments which would decrease the usefulness of the signal. This paper therefore introduces design of a LNA receiver sensitivity of -121.84dBm in a two-stage Bipolar Junction Transistor (BJT) amplifier at 2.2GHz.

The Sensitive LNA design has a gain of 12dB, taking into consideration the various noise levels for these design and the system remains unconditionally stable.

Keywords
Low Noise Amplifier (LNA), Sensitivity, gain

1. INTRODUCTION
The smallest possible signal that can be picked up by the receiver is the reference for the receiver's sensitivity.

Similarly, the largest signal that can be picked up by the receiver establishes an upper power level limit that can be handled by the system while preserving voice or data quality.

Since the Low Noise Amplifier provides first level of amplification of the received signal at the system's antenna, the sensitivity of the system is very important considering the signal to noise ratio, channel interference and the antenna's frequency of operation.

The dynamic range of the receiver, which is the difference between the largest possible received signal and the smallest possible received signal, defines the quality of the receiver chain.

Additionally, for large signal levels, the LNA amplifies the received signal without introducing any distortions, hence eliminating channel interference [4].

The sensitivity of a LNA design is crucial in today's wireless communication.

The front end low noise amplifiers have been widely used in many applications including wireless personal communication systems [8].

2. METHODOLOGY
The following procedures were used to design the sensitive LNA;

2.1 Transistor Selection
The transistor selection is the first and most important step in this LNA design. The transistor must exhibit high gain, low noise figure, high IP3 performance at the lowest possible current consumption, while preserving relatively easy matching at the proposed frequency of operation, and at collector emitter voltage (Vce) and collector (Ic) levels will produce the most optimal performance. The BJT BRF193 silicon transistor by Siemens was chosen after evaluating its characteristics on the datasheet.

2.2 DC Analysis
The DC bias circuit exhibit stable thermal performance and does not increase complexity of the design and preserves smallest possible size for the overall Sensitive LNA as shown in figure 1.

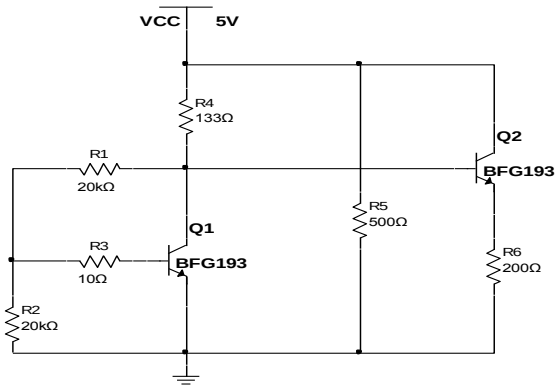

Fig 1: DC analysis of the LNA Design

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2.2.1 DC analysis of Stage I

The V_{BE} = 0.7V, β = 125 are obtained from the data sheet of the BFG 193 Silicon Transistor;

The $V_{BB} = \left(\frac{R2}{R1+R2}\right) Vcc$ is taking across Q1 in figure 1

Insert the values of $R_1 = 20 \times 10^3\Omega$,

$R_2 = 20 \times 10^3\Omega$, $R_3 = 10\Omega$, Vcc = 5V

The voltage divider bias method was applied across the base of Q1 as shown in figure 1

$$VBB = \left(\frac{20\times10^3}{20\times10^3+20\times10^3}\right)5 = 2.5V$$

Looking at a closed loop around I_b in the first stage transistor Q1 $VBB = IbR2 + IbR3 + VBE$

$$2.5 = 20 \times 10^3\ (\text{Ib}) + 10\ (\text{Ib}) + 0.7$$

$$Ib = \frac{2.5-0.7}{20\times10^3+10} = 8.9955 \times 10^{-5} Amp$$

$Ic1 = \beta Ib$ (Ic – collector current, Ib - base current, Ie – emitter current)

$$Ic1 = 125 \times 8.9955 \times 10^{-5} = 11.2\ mAmp$$

$Ie = Ic + Ib$

$$Ie = 11.2 \times^{-3} + 8.9955 \times 10^{-5} = 11.3 mAmp$$

$VR4 = Ic1 \times R4$

$$VR4 = 11.2 \times^{-3} \times 133 = 1.49V$$

$Vcc = VR4 + Vce$

$Vce = Vcc - VR4 = 5 - 1.49 = 3.51V$

$I_E = 11.3mAmp$, $I_c =$ $11.2mAmp$, *Internal Signal Resistance* $(re_i^i = \frac{25mV}{I_E})$

V_f is parallel to V_{cc} = 5V, R_5=R_f = 500Ω

$V_f = I_{cf} \times R_5$

$$I_{cf} = \frac{5}{500} = 10mAmp$$

2.2.2 DC analysis of Stage II

The Second stage which is transistor Q2 from figure 1 has a very small base current I_b . It is assumed to be equal to the base current at the first stage. (I_b=$8.9955 \times 10^{-5} Amp$)

Taking a close loop at the second amplifier stage;

$Vce = Vbe + IeRe$

$3.51 = 0.7 + Ie \times 200$

$$Ie = \frac{3.51-0.7}{200} = 14.05mAmp$$

$Ie = Ic + Ib$

$Ic2 = Ie - Ib = 14.05 \times^{-3} - 8.9955 \times 10^{-5} =$ $13.96mAmp$

Total Current is $IcT = Ic1 + Icf + Ic2$

$IcT = 11.2mAmp + 10mAmp + 13.96mAmp =$ $35.16mAmp$

Hence, V_{ce} = 3.51V; I_c = 35.16mAmp; I_b = $8.9955 \times 10^{-5} Amp$

2.3 Circuit Stabilization

The Instabilities of a system are primarily caused by three phenomena: internal feedback of the transistor, external feedback around the transistor caused by external circuit, or excess of gain at frequencies outside of the band of operation [2].

Hence a sensitive LNA must be unconditionally stable.

The two main methods existing in S-parameter stability analysis are being used for the design of this circuit namely; numerical and graphical.

2.3.1 Numerical Analysis

$$\Delta = S_{11} * S_{22} - S_{21} * S_{12}$$

$$K = \frac{1-{S_{11}}^2-{S_{22}}^2+\Delta^2}{2(S_{21}*S_{12})}$$

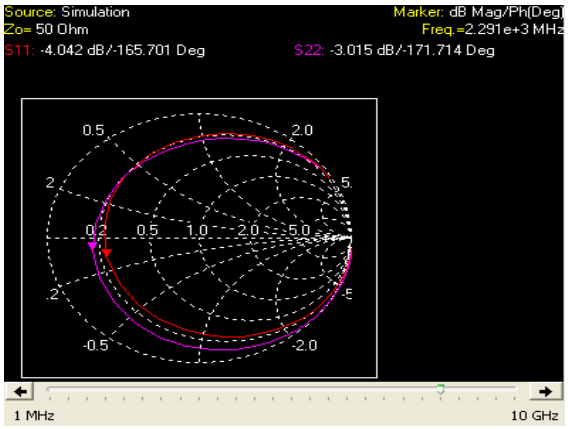

Fig 2: Multisim simulation of LNA Design S-Parameter

S11 = 0.701; S12 = 0.024; S21 = 1.029; S22 = 0.749

$$\Delta = S_{11} * S_{22} - S_{21} * S_{12}$$
$$= 0.701 * 0.749 - 1.029 * 0.024$$
$$= 0.50$$

$$K = \frac{1 - {S_{11}}^2 - {S_{22}}^2 + \Delta^2}{2(S_{21} * S_{12})}$$
$$= \frac{1 - 0.701^2 - 0.749^2 + 0.50^2}{2(1.029 * 0.024)}$$
$$= 4.0$$

The LNA system is unconditionally stable at 2.2 GHz since k = 4.0 using the S – parameter numerical analysis.

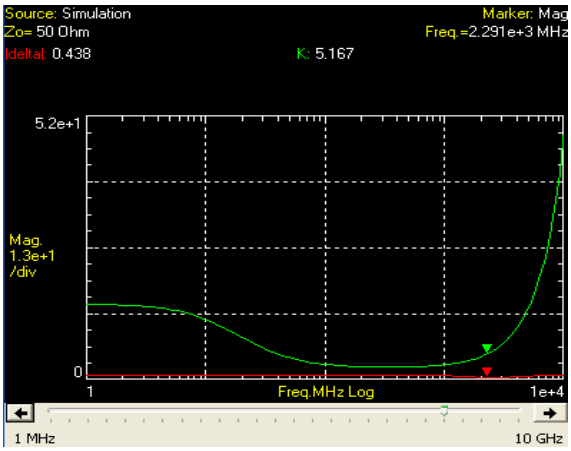

Fig 3: LNA design stability

The S parameter graphical analysis shows that K = 5.167 as shown in figure 3 above. This confirms that the system is unconditionally stable at the 2.2GHz frequency of operation.

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The K factor of the design for sensitive LNA is greater than unity, hence the circuit will be unconditionally stable for any combination of source and load impedance.

2.4 AC Equivalent Circuit

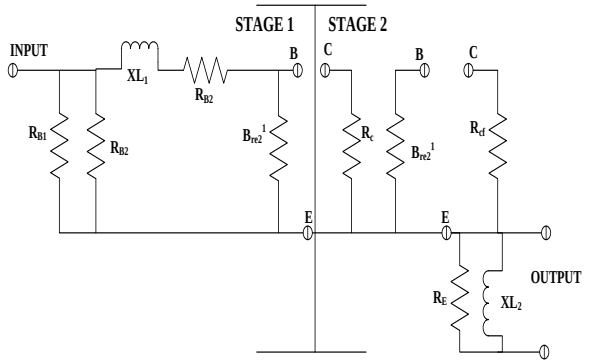

Fig 4: AC analysis of LNA design

The figure 4 show the AC equivalent circuit of the design of a sensitive low noise amplifier.

The stage 1 and stage 2 as shown in figure 4 has been analysed from section 2.4.1 to 2.4.6

2.4.1 Stage 1

$Internal\ Signal\ Resistance;\ re_i^i = \frac{25mV}{I_E} \quad I_E = 11.3mAmp,\ I_C = 11.2mAmp$

$re_i^i = \frac{25mV}{11.3mA} = 2.21V$

$Transconductance(g) = \frac{I_E}{V_T} = \frac{11.2mA}{25mV} = 0.45$

Input Resistance (r_π) = $\beta r_{e^i} = 125 \times 2.21 \cong 276\Omega$

$R_{B_i} // R_{B_2} = 20k//20\text{k} = \frac{20 \text{ x } 10^3 \times 20 \text{ x } 10^3}{20 \text{ x } 10^3 \times 20 \text{ X } 10^3} = 10\ k\Omega$

$X_{L_1} = 2\pi fL = 2\pi(2.2\ x\ 10^9)(3.3\ x\ 10^{-9}) = 45.62\Omega$

Input Impedance; $Z_{in} = (R_{B_i} // R_{B_2})//(X_{L_1} + R_{B_3} + \beta r_{e^i})$

$Z_{in} = (10 \text{ x } 10^3)//(45.62 + 10 + 276.55) = 10 \text{ x } 10^3//332.17 = 321.49\Omega$

$R_c = 133\Omega\ ;\ B_r{}^i{}_2 = 125(re_2^1) = 123 \times 1.78 = 222.5$

Output Impedance; $Z_{out} = 133//22.5 = \frac{133 \times 222.5}{133 \times 222.5} = 83.24$

$A_{v1} = \frac{Z_{out}}{r_{in}} = \frac{83.24}{321.49} = 0.26$

$C_\pi = \frac{g_m}{2\pi f_T} - C_\mu$

$C_\pi = \frac{0.45}{2\pi \times 2.2 \times 10^9} - 0.68 \times 10^{-12} = 3.19 \times 10^{-11} =$ 31.9pF

2.4.2 Stage II

$I_c = 13.96mA\ , I_e = 14.05mA\ , C_\mu = 0.68$ pF

$Transconductance(g) = \frac{I_E}{V_T} = \frac{14.05mA}{25mV} = 0.56$

$re_2^i = \frac{25mV}{I_E} = \frac{25 \times 10^{-3}}{14.05 \times 10^{-3}} = 1.78\Omega$

$\beta r_{e_i^i} = 125\ x\ 1.78 = 222.5$

$r_o = X_{L2} // R_E = 37.32//200$

$XL_2 = 2\pi f_L = 2\pi \text{ x } 2.2 \text{ x } 10^9 \text{ x } 2.7 \text{ x } 10^{-9} = 37.32\Omega$

$r_o = X_{L2} // R_E = 37.32//200$

$r_{out} = \frac{37.32 \times 200}{37.32 \times 200} = 31.45\Omega$

$A_v = \frac{r_o}{r_{e_2^1}} = \frac{31.45}{1.78} = 17.67$

2.4.3 Voltage Gain

$A_v = A_{v_1} \times A_{v_2} = 0.26 \times 17.67 = 4.59$

2.4.4 In Decibel

$20\log 4.59 = 13.24\text{dB}$

$C_\pi = \frac{g_m}{2\pi f_T} - C_\mu$

$C_\pi = \frac{0.56}{2\pi \times 2.2 \times 10^9} - 0.68 \times 10^{-12} = 39.8 \times 10^{-11} = 39.8\text{pF}$

2.4.5 Output Third Order Intercept Point (IP3)

$OIP3 = 10 * \log(V_{ce} * I_c * 5)\ [dBm] = 10 * \log(3.51 * 35.15 \times 10 - 3 \times 5 = -2.1dBm$

2.4.6 Input Third Order Intercept Point (IP3)

$IIP3 = OIP3 - Gain[dBm] = -2.1 - 13.24 = -15.34dBm$

2.5 Calculating the various capacitors in the High Sensitive LNA design

The figure 1 and figure 4 showing the dc and ac analysis respectively are critically analysed before the addition of the coupling and decoupling capacitors.

The X_c, at the lowest frequency is calculated to be equal to one-tenth or less of the series impedance being driven by the signal passing through the capacitor. The coupling capacitor between the stages have an impedance of one-tenth of Z_{in} of the stage being driven. The output coupling capacitor have an impedance of one-tenth of *RL*. The signal passing through the input coupling capacitor is driving Z_{in} of the first stage of the circuit, and the impedance of the coupling capacitor is one-tenth of Z_{in}. All th value of capacitors derived were used for the design of the high sensitive LNA as shown in figure 6.

At C_1

The input resistance at C_1 is 321.49Ω;

Hence;

$R_{c1} = \frac{1}{10} of\ 321.49 = \frac{1}{10} \times 321.49 = 32.149\Omega$

$C_1 = \frac{1}{2\pi R_{c1} F} = \frac{1}{2\pi \times 32.149 \times 2.2 \times 10^9} = 2.3pF$

At C2

The input resistance at C_2 is 321.49Ω;

Hence;

$R_{c2} = \frac{1}{10} of\ 321.49 = \frac{1}{10} \times 321.49 = 32.149\Omega$

$C_2 = \frac{1}{2\pi R_{c2} F} = \frac{1}{2\pi \times 32.149 \times 2.2 \times 10^9} = 2.3pF$

AT C3

The resistance at C_3 is 500Ω;

Hence;

$R_{c3} = \frac{1}{10} of\ 500 = \frac{1}{10} \times 500 = 50\Omega$

$C_3 = \frac{1}{2\pi R_{c3} F} = \frac{1}{2\pi \times 50 \times 2.2 \times 10^9} = 1.45pF$

AT C4

The resistance at C_3 is 31.45Ω;

Hence;

$R_{c4} = \frac{1}{10} of\ 31.45 = \frac{1}{10} \times 31.45 = 3.145\Omega$

$C_4 = \frac{1}{2\pi R_{c4} F} = \frac{1}{2\pi \times 3.145 \times 2.2 \times 10^9} = 23pF$

2.5.1 Higher Frequency Boarder for Coupling and Bypass Capacitor

The critical frequency (f_c) for the circuit is the frequency that produces a capacitive reactance that is equal to the total resistance in the circuit {X_c=R}. Note that the coupling capacitor acts as a short at high frequency, meaning that 10 times as high as the critical frequency {f_H>10f_c}.

$$f_c = \frac{1}{2\pi Rc};$$

$R_B = R_{B1} // R_{B2} = 20k\Omega // 20k\Omega = 10k\Omega$

(a) At 2.3pf; $f_c = \frac{1}{2\pi(10 \times 1000) \times (2.3 \times 10^{-12})} = 6.9$MHz

f_H = 10f_c = 10 x 6.9MHz = 69MHz

As long as the generator (2.2GHz) is above 69MHz; the capacitor act as AC short circuit.

(b) At 2.3pf and $R_B = 10\Omega$; $f_c = \frac{1}{2\pi Rc}$; $\frac{1}{2\pi(10)(2.3 \times 10^{-12})} =$ 6.9GHz

f_H = 10f_c = 10 x 6. $9 \times 10^9 Hz$ = 69GHz

Since the generator (2.2GHz) is lower than 69GHz; the capacitor acts as AC open circuit.

(c) At 1.45pf; R=500Ω; $f_c = \frac{1}{2\pi(500)(1.45 \times 10^{-12})} = 220$MHz

f_H = 10f_c = 10 x 220MHz = 2.2GHz

Since the generator (2.2GHz) is equivalent to 2.2GHz; the capacitor acts as AC open circuit.

(d) At 23pf; R=200Ω; $f_c = \frac{1}{2\pi Rc} = \frac{1}{2\pi(200)(23 \times 10^{-12})} = 35$MHz

f_H = 10f_c = 10 × 35MHz = 350MHz

Since the generator (2.2GHz) is higher than 350MHz; the capacitor act as AC short circuit.

2.6 Noise Figure Considerations

In receiver applications, it is often required to have a preamplifier which has low noise figure as minimum as possible, since the first stage of a receiver front end has the dominant effect on the noise performance of the overall system. The noise figure parameter, N, is given by

$N.F = \frac{F - F_{min}}{4R_N/Z_0} \left|1 + \Gamma_{opt}\right|^2$

Where, the quantities F_{min}, Γ_{opt} and RN are the characteristics of the transistor being used and are called the noise parameters of the device [1]

From the BFR193 datasheet, it has already verified that N.F = 2.1 at 1.8 GHz.

2.6.1 Thermal Noise

Thermal noise voltage across an input resistor (R_{c1}) considering the frequency of operation (f), absolute temperature (T) and Boltzmann's Constant (K) is given by [5],

$$V_t = \sqrt{4KTR\Delta f}$$
$$= \sqrt{4 \times 1.38 \times 10^{-23} \times 300 \times 321.49 \times 2.2 \times 10^9}$$
$$= \sqrt{1.17 \times 10^{-8}} = 1.08 \times 10^{-4} V$$

It has been concluded that the total noise voltage generated by a resistor is a function of the temperature and the total shunt capacitance (C_1) across the resistor. Hence,

$$V_t = \left[4KT \int_0^\infty \frac{Rdf}{1 + (2\pi fRC)^2}\right]^2 = \sqrt{\frac{kT}{c1}}$$
$$= \sqrt{\frac{1.38 \times 10^{-23} \times 300}{2.3 \times 10^{-12}}} = \sqrt{1.8 \times 10^{-9}}$$
$$= 4.2 \times 10^{-5} V$$

2.6.2 Shot Noise

The shot noise generated by a device is modeled by a parallel noise current source [6]. The *Ib* is the base current,

$$I_{sh} = \sqrt{2qIb\Delta f}$$
$$= \sqrt{2 \times 1.6 \times 10^{-19} \times 8.9955 \times 10^{-5} \times 2.2 \times 10^9}$$
$$= \sqrt{6.33 \times 10^{-14}} = 2.5 \times 10^{-7} Amp$$

2.6.3 Flicker Noise

The imperfect contact between two conducting materials causes the conductivity to fluctuate in the presence of a dc current (I^m is assumed as *Ib)* and this phenomenon generates what is called flicker noise [7].

$$I_f = \sqrt{\frac{K_f I^m \Delta f}{f^n}}$$
$$= \sqrt{\frac{1 \times 10^{-19} \times 8.9955 \times 10^{-5^1} \times 2.2 \times 10^9}{2.2 \times 10^{9^1}}}$$
$$= \sqrt{8.9955 \times 10^{-24}} = 3 \times 10^{-12} Amp$$

2.6.4 The BJT noise model

Noise specifications for BJT's commonly give measured values for V_n and I_n for the V_n-I_n amplifier noise model as shown below;

$$V_n = \sqrt{4kTr_x\Delta f + 2kT\frac{V_T}{I_C}\Delta f}$$
$$= \sqrt{\begin{matrix}4 \times 1.38 \times 10^{-23} \times 300 \times 321.49 \times 2.2 \times 10^9 + \\ 2 \times 1.38 \times 10^{-23} \times 300 \times \frac{0.0259}{35.16 \times 10^{-3}}\end{matrix}} \times 2.2$$
$$\times 10^9 = \sqrt{1.17 \times 10^{-8}} = 1.08 \times 10^{-4} V$$

$$I_n = \sqrt{2qI_B\Delta f + \frac{k_f I_B}{f}\Delta f + \frac{2qI_C}{\beta^2}\Delta f}$$
$$= \sqrt{\begin{matrix}2 \times 1.6 \times 10^{-19} \times 8.9955 \times 10^{-5} \times 2.2 \times 10^9 + \\ \frac{1 \times 10^{-19} \times 8.9955 \times 10^{-5^1} \times 2.2 \times 10^9}{2.2 \times 10^{9^1}} + \\ \frac{2 \times 1.6 \times 10^{-19} \times 35.16 \times 10^{-3} \times 2.2 \times 10^9}{125^2}\end{matrix}}$$
$$= \sqrt{6.33 \times 10^{-14} + 8.9955 \times 10^{-24} + 1.584 \times 10^{-15}}$$
$$= \sqrt{6.49 \times 10^{-14}} = 2.55 \times 10^{-7} Amp$$

3. LNA SENSITIVITY

$F = F_1 + \frac{F_2 - F_1}{G_1} + \frac{F_3 - F_1}{G_1 G_2} + \cdots + \frac{F_N - F_1}{G_{N!}}$

F_1 is the thermal noise generated at the input resistance in section 2.6.1

$F_1 = 10\log(1.08 \times 10^{-4} V) = 10 \times -3.967 = -39.67$dB

F_2 is the noise generated at the first stage transistor which is 2.1dB from the datasheet

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F_3 is the noise generated at the second stage transistor which is 2.1dB from the datasheet

F_4 is the thermal noise generated at the output resistance

$$F_4 = 10\log(3.38 \times 10^{-5}V) = 10 \times -4.47 = -44.7\text{dB}$$

$$F = -39.67 + \frac{2.1 - -39.67}{13.26} + \frac{2.1 - -39.67}{13.26 \times 13.26} + \frac{-44.7 - -39.67}{13.26 \times 13.26 \times 13.26} = -36.28\text{dB}$$

Assuming from Nomograph of signal – noise ratio (SNR) as a function of probability of detection is at 98% which is equivalent to 12dB.

Quality factor (Q) = $\frac{F_0}{BW}$

Where F_o is Operating Frequency and BW is bandwidth.

A good signal quality factor varies from 10 – 50. Hence, assume for a good signal quality to be 50 for this design.

BW = $\frac{2.2 \times 10^9}{50}$ = 44 MHz

$$R_x\_Sen(dBm) = -174 + 10logBW + SNR + F \quad [3]$$

The receiver sensitivity of the design low noise amplifier is;

$$R_x\_Sen(dBm) = -174 + 10\log(44 \times 10^6) + 12\text{dB} + (-38.39\text{dB}) = \mathbf{-121.84dBm}$$

In achieving a high sensitive receiver, the maximum Power Transfer theorem must be obeyed.

Hence,

P = KTB = -174dBm/Hz (The reference noise level in a 1Hz, at room temperature)

where;

K = Boltzmann's Constant = 1.38×10^{-23}

T = 300K

B = Bandwidth

Receiver sensitivity (Rx) = -174 + 10logB + SNR + N.F (1)

SNR = Signal to Noise ratio

N.F = Noise Figure

SNR = $10log\frac{S_i}{N_i}$ (dB) (2)

Si = Input signal

Ni = Input noise

N.F = $10log\frac{S_i/N_i}{S_o/N_o}$ = $10log\frac{SNR_i}{SNR_o}$ (3)

SNRi = Input signal to noise ratio

SNRo = Output signal to noise ratio

From Shannon – Hartley's theorem [9];

$C = B\log_2(1 + \frac{S_i}{N_i})$

$C = \frac{1}{\log_{10} 2} B\log_{10}(1 + \frac{S_i}{N_i}) = 3.32B\log_{10}(1 + \frac{S_i}{N_i})$

C = Channel capacity (bits/sec),

Making B the subject of the formula;

$$B = \frac{C}{3.32\log_{10}(1+\frac{S_i}{N_i})} \quad (4)$$

Substitute for equation (2), (3), (4) in equation (1)

$$Rx = 10\log_{10}\frac{C}{3.32\log_{10}(1+\frac{S_i}{N_i})} + 10log\frac{S_i}{N_i} + 10log\frac{S_i/N_i}{S_o/N_o} - 174$$

Note $\log_{10} A + \log_{10} B = \log_{10} A \times B$

$$Rx = 10\log_{10}\frac{C}{3.32\log_{10}(1\times\frac{S_i}{N_i})} \times 10log\frac{S_i}{N_i} \times 10log\frac{S_i/N_i}{S_o/N_o} - 174$$

$$Rx = 10\frac{C}{3.32} \times \frac{S_i/N_i}{S_o/N_o} - 174 = 3.012 \times C \times \frac{S_i/N_i}{S_o/N_o} - 174$$

Rx = 3.012CN.F – 174 (5)

Hence, it has been analyzed that the two major trade off for a high level of LNA sensitivity is the channel capacity (C) and noise figure (N.F) as shown in equation (5).

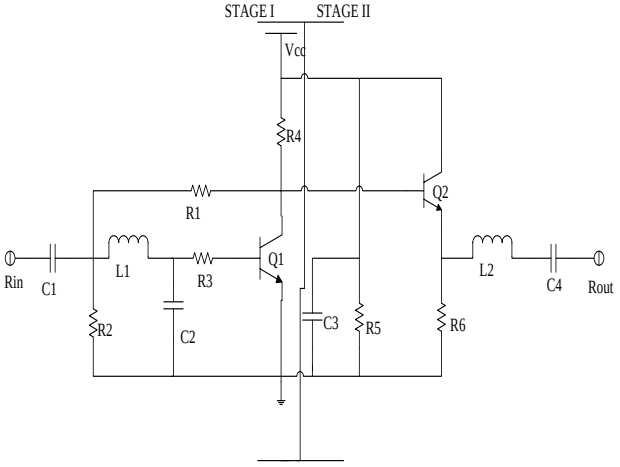

Fig 6: A High Sensitive LNA Design at 2.2 GHz frequency

4. SIMULATION RESULT

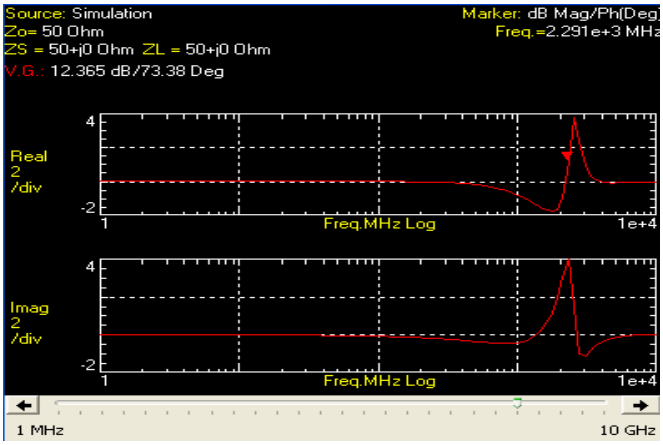

Fig 7: LNA Gain

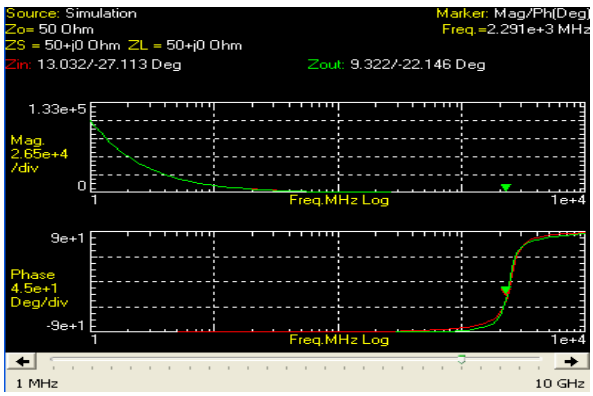

Fig 8: LNA Design input and output impedance

4.1 Result and Discussion

The result derived after mathematically analyzing the dc and ac analysis from section 2.1 to 2.5 shows that the Sensitive LNA system is properly designed for a high frequency amplifier. The dc circuit analysis is shown in figure 1 and the ac circuit analysis is shown in figure 4. Table 1 gives a detail comparism of the mathematical analysis been compared with the simulation results obtained from figure 2, 3, 7 and 8.

Although the simulation results and mathematical analysis varies but it shows that the system is unconditionally stable as shown in figure 2 and 3.

The sensitivity of the LNA system as shown in section 3 shows that the system is high sensitive and the trade off in acquiring a high sensitive LNA depends on the Channel capacity and Noise Figure as shown in equation 5.

The noise generated from both the transistor and the components on the circuit were analysed in section 2.6. The system noise must be minimal so that adequate signal propagated can be received with minimal signal to noise ratio.

All these various parameters has been consider and used in designing the High frequency and high sensitive low noise amplifier as shown in figure 6.

Table 1: Comparism of simulated and mathematical results

FREQUECY (2.2GHz)	SIMULATION	CALCULATION
GAIN	12.37dB	13.26dB
I_c	34.6mA	35.16mA
V_s	5V	5V
V_{ce}	3.54V	3.51V
Sensitivity		-121.84dBm

More also, the design of a high sensitive LNA for wireless communication at high frequency considering the gain of the amplifier is determined by the quality of the RF transistor used in the design.

This sensitive high frequency LNA design is based on 50 Ω input and output impedance.

5. CONCLUSION

This design is aim at developing a high sensitive LNA at high frequency of operation. This could be used for any wireless communication devices.

The efficiency of this design is at 2.2 GHz frequency considering the gain, system stability, input matching, output matching, signal to noise ratio and the sensitivity of the designed LNA.

The two major trade off for a high level of the LNA receiver sensitivity are the channel capacity and noise figure as shown in equation 5. This was accounted for during the design.

The mathematical relationship between Shannon's Hartley, quality factor, Boltzmann's constant, room temperature, signal to noise ratio and noise figure of the system has been studied and applied to realizing the high sensitive low noise amplifier.

The amplification has a gain of 12dB at the center frequency of 2.2GHz with a receiver sensitivity of -121.84dBm.

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